

MS-7676

UATX Ver:11

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH

OnBoard Chipset:

Clock Gen:IDT 4106

HD Audio Codec:RTL892

LAN:RTL 8111E 10/100/1000

SIO:FIN71889AD

Flash ROM: 64 Mb SPI (PCH)* 2

Main Memory:

DDR3 (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X4) Slot * 1

PCI Express (X1) Slot * 2

PWM:

Controller:VRD12 UPI6234 (6+2-Phase)Dr.MOS

CPU+GPU

Controller:uP6113 Dr.MOS

CPU VTT CPU SA

Controller:uP6103A

DDR PCH

ACPI:

UPI

Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

SATA3.0X1 + e-SATA X1(MARVELL)

USB2.0 RearX4 Front x8(PCH)

USB3.0 RearX2 (NEC uPD720200)

1394 Controller - VT6315N-CE

D-SUB *1

DVI-D PORT*1

HDMI *1

TPM Header *1

COM Header *1

on BOARD BUZZER

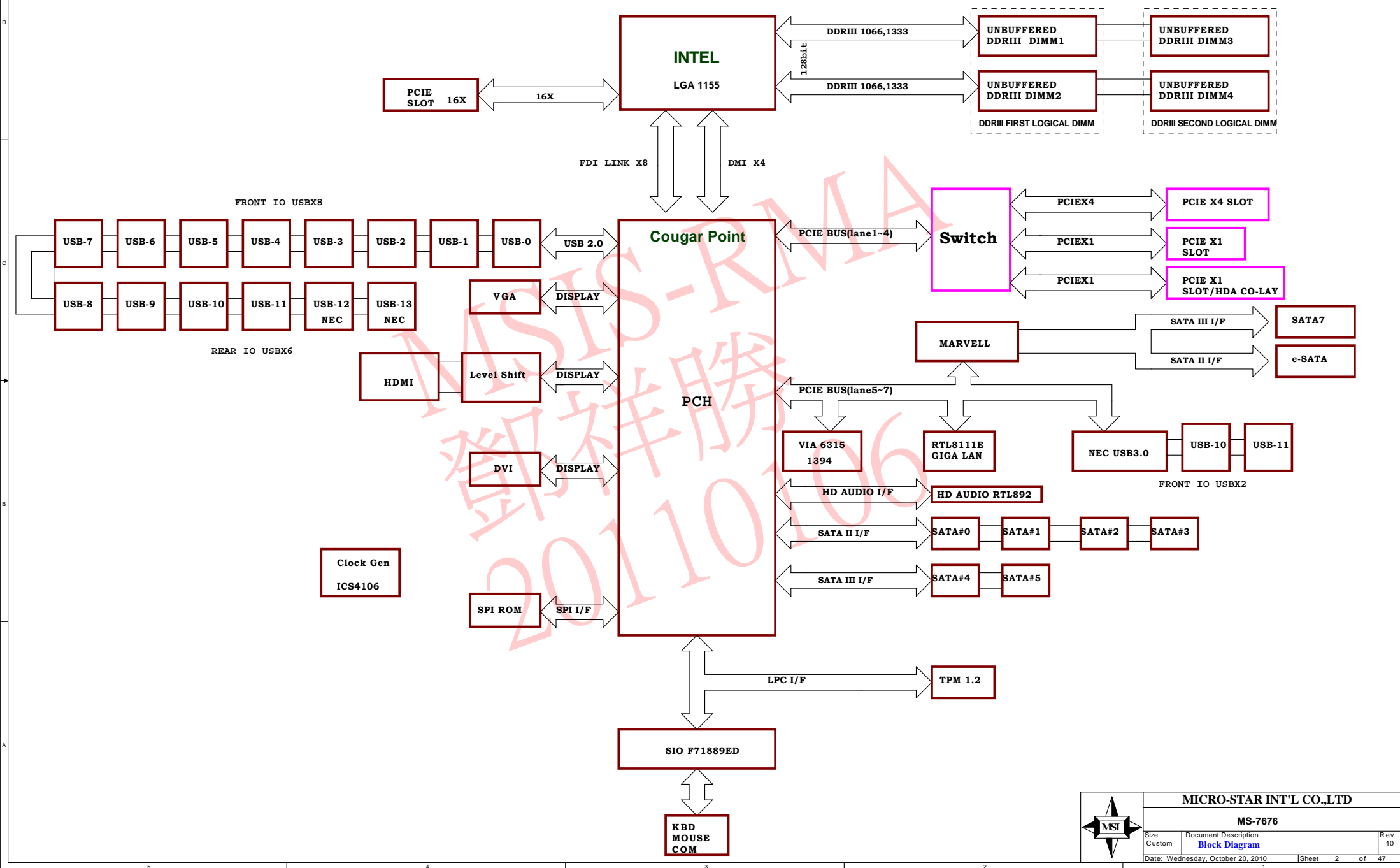
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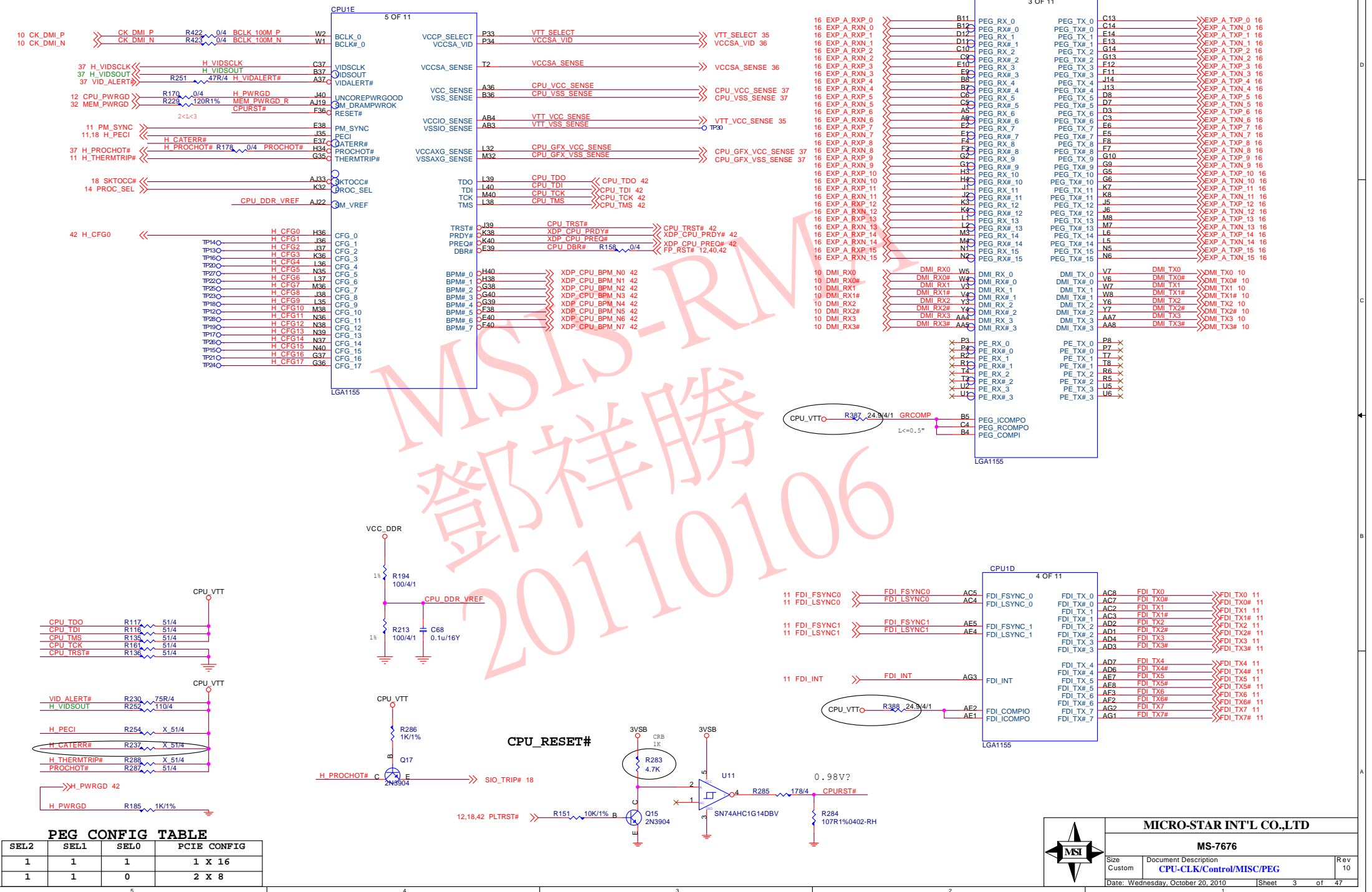


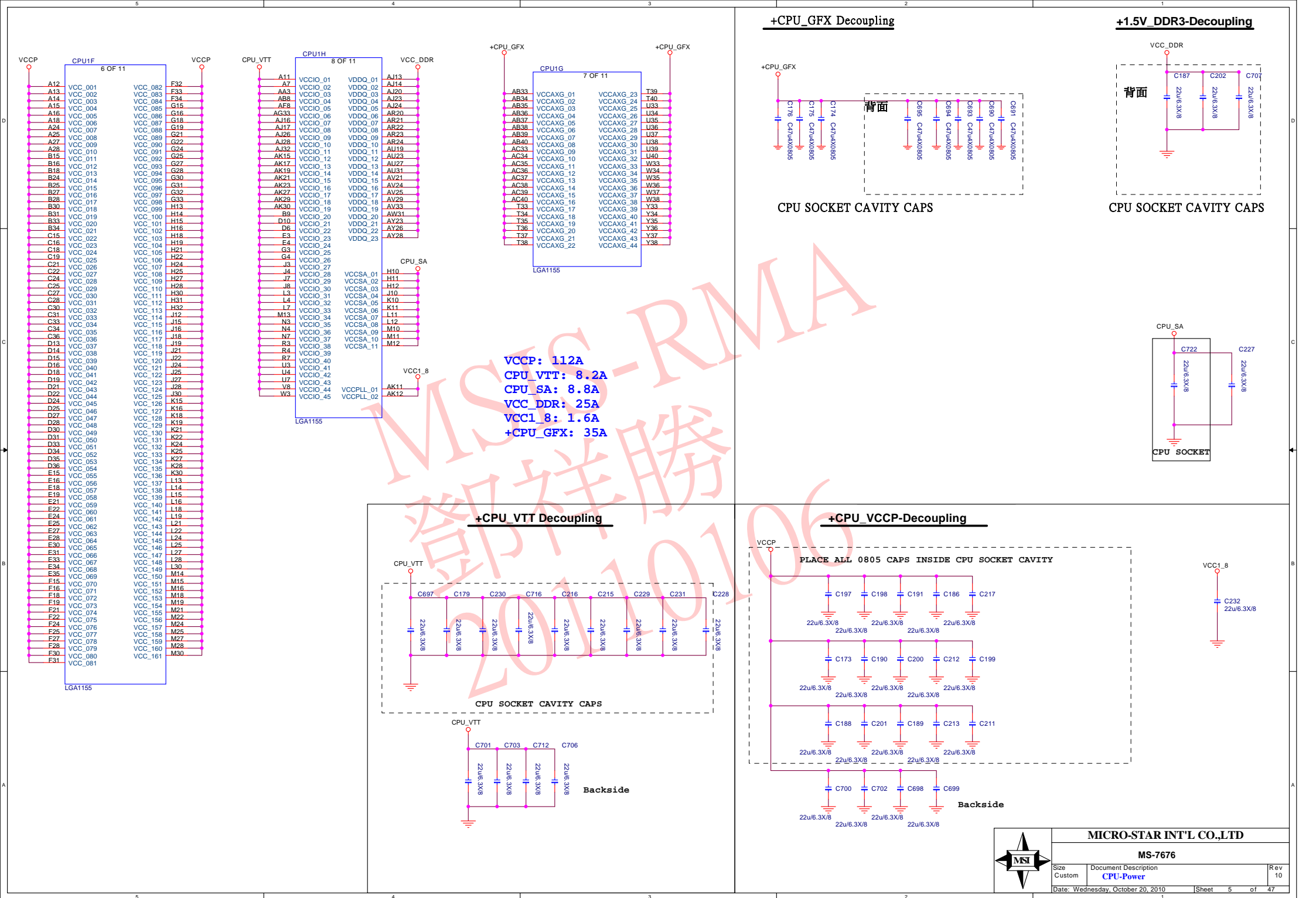
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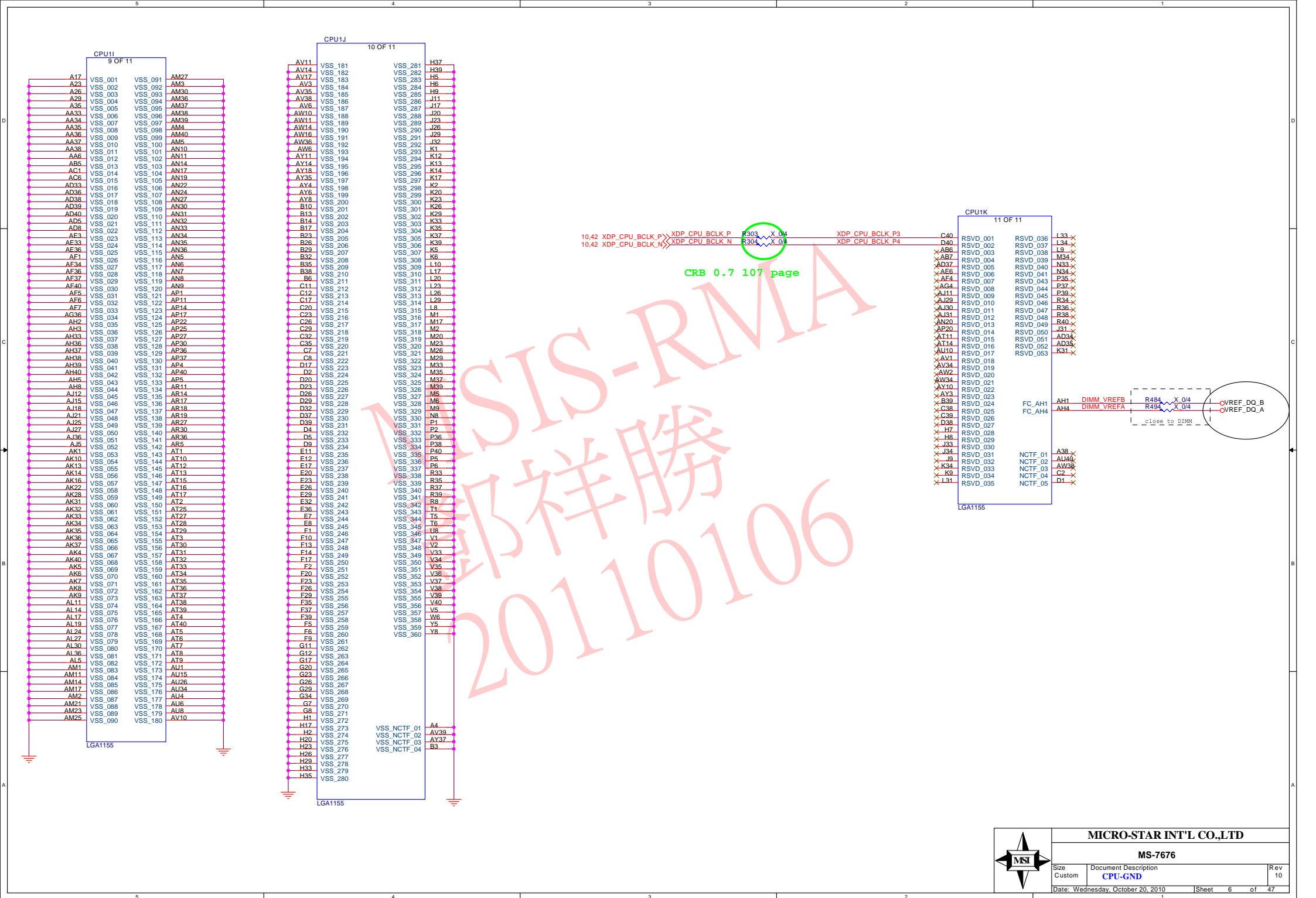
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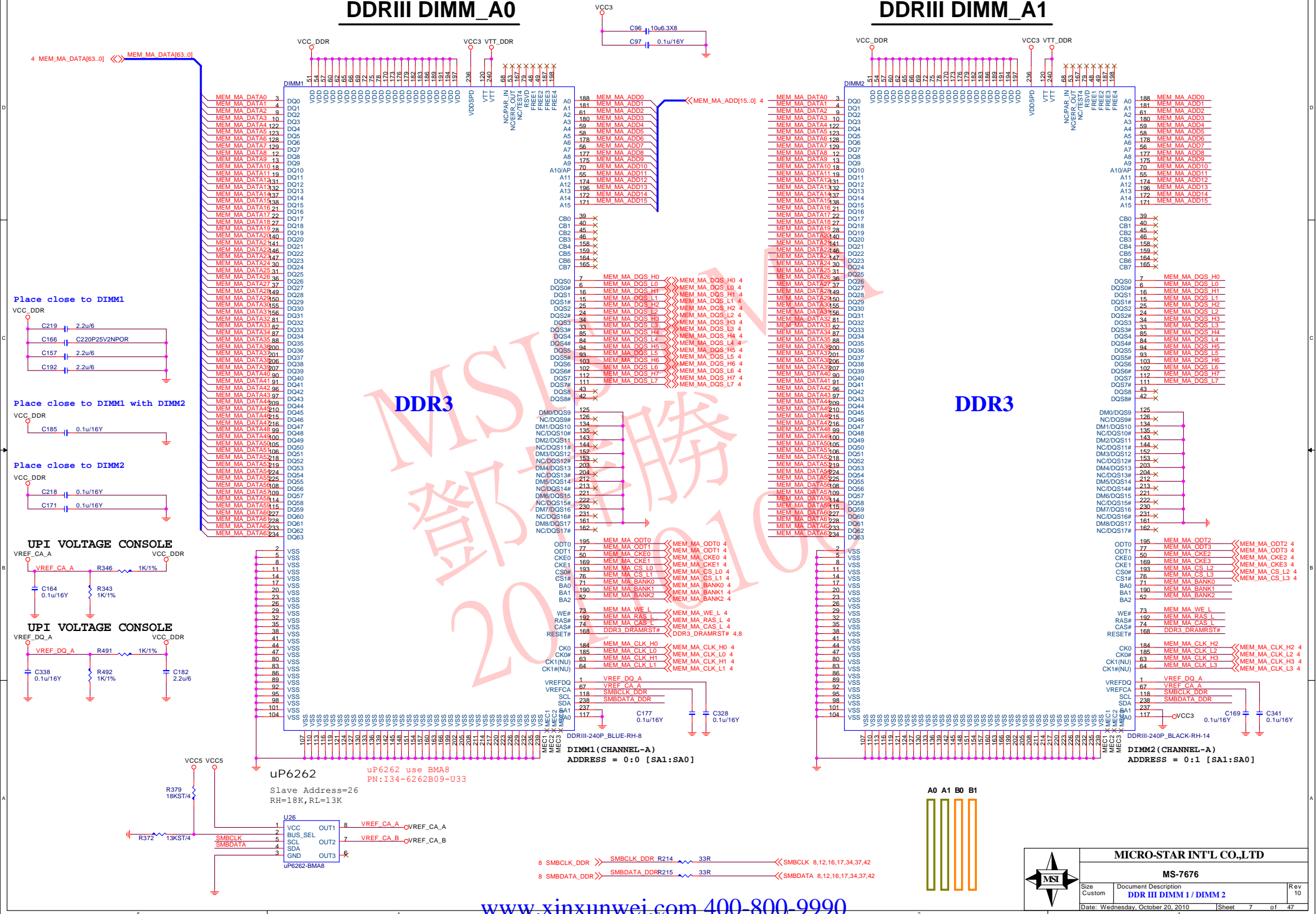




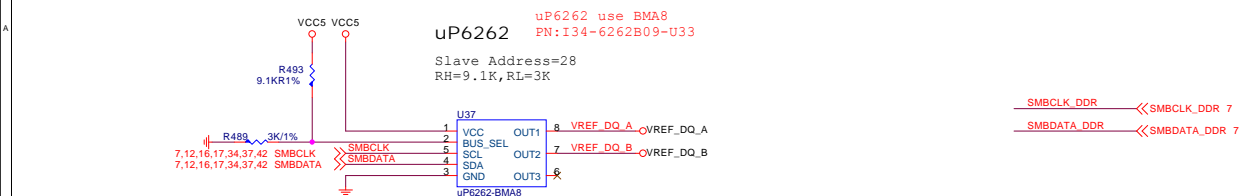
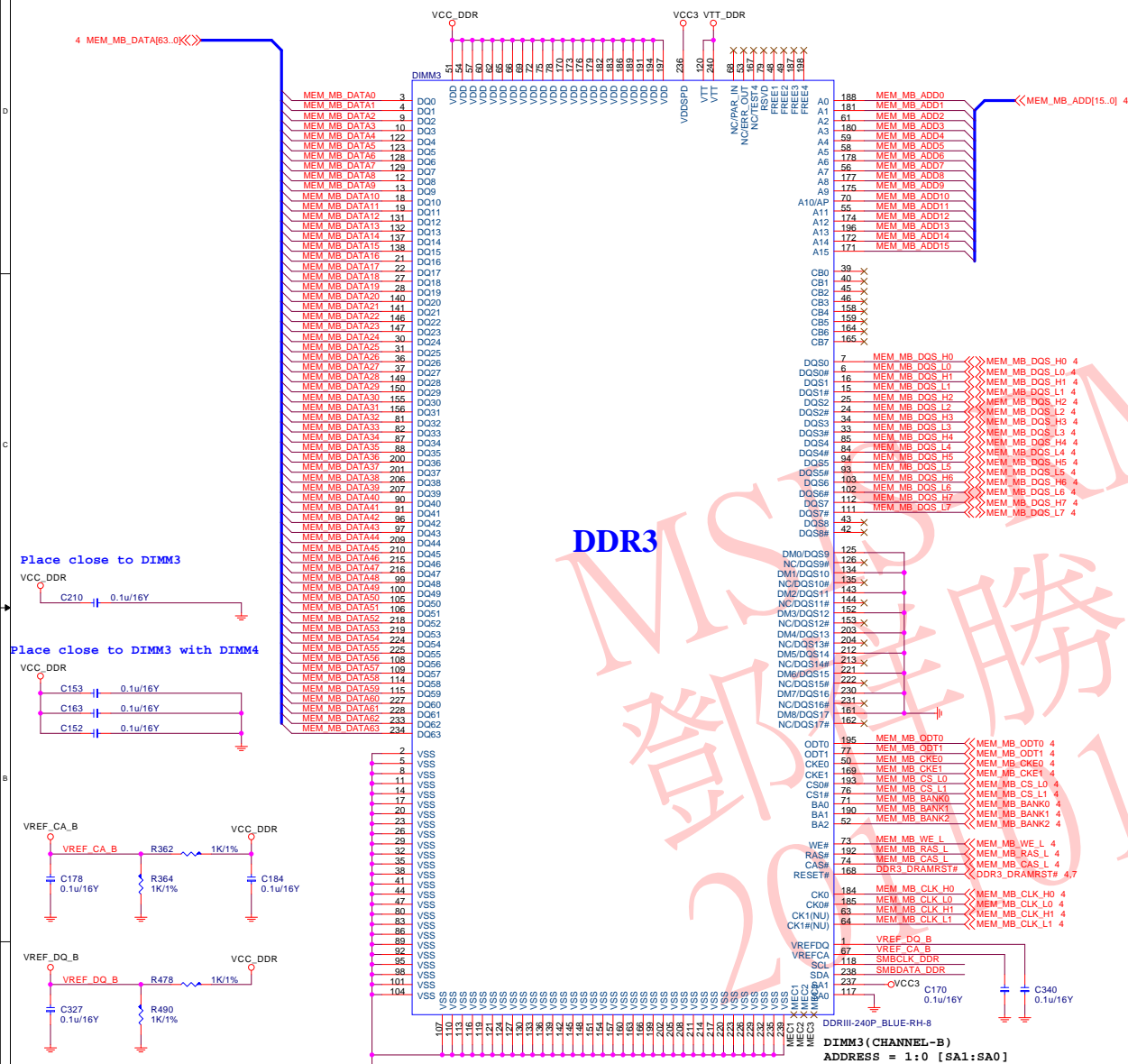


DDRIII DIMM_A0

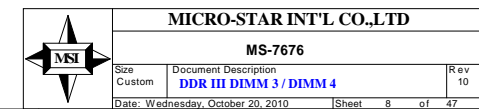
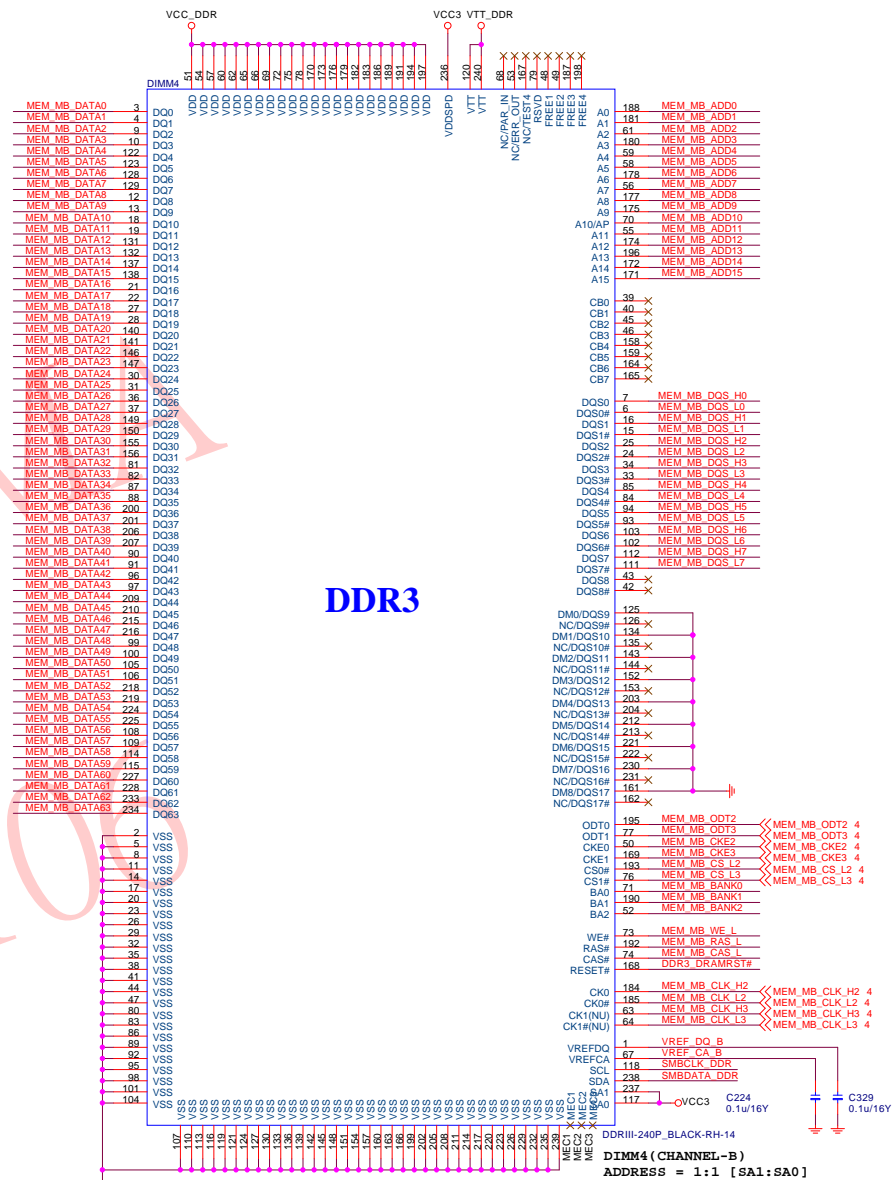
DDRIII DIMM_A1



DDRIII DIMM_B0



DDRIII DIMM_B1



MSIS-RMA
鄧祥勝
20110106



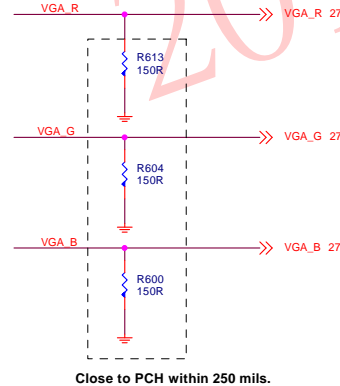
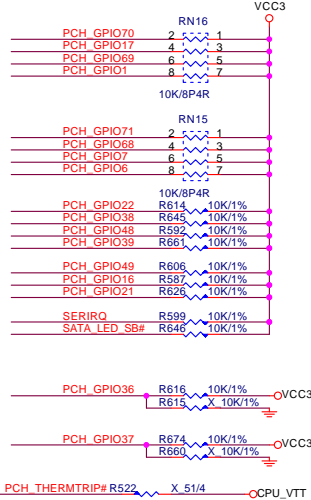
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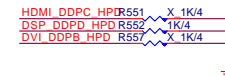


Pull HIGH for PCH

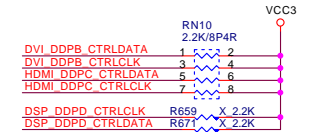


Close to PCH within 250 mils.

No VGA(pull down)



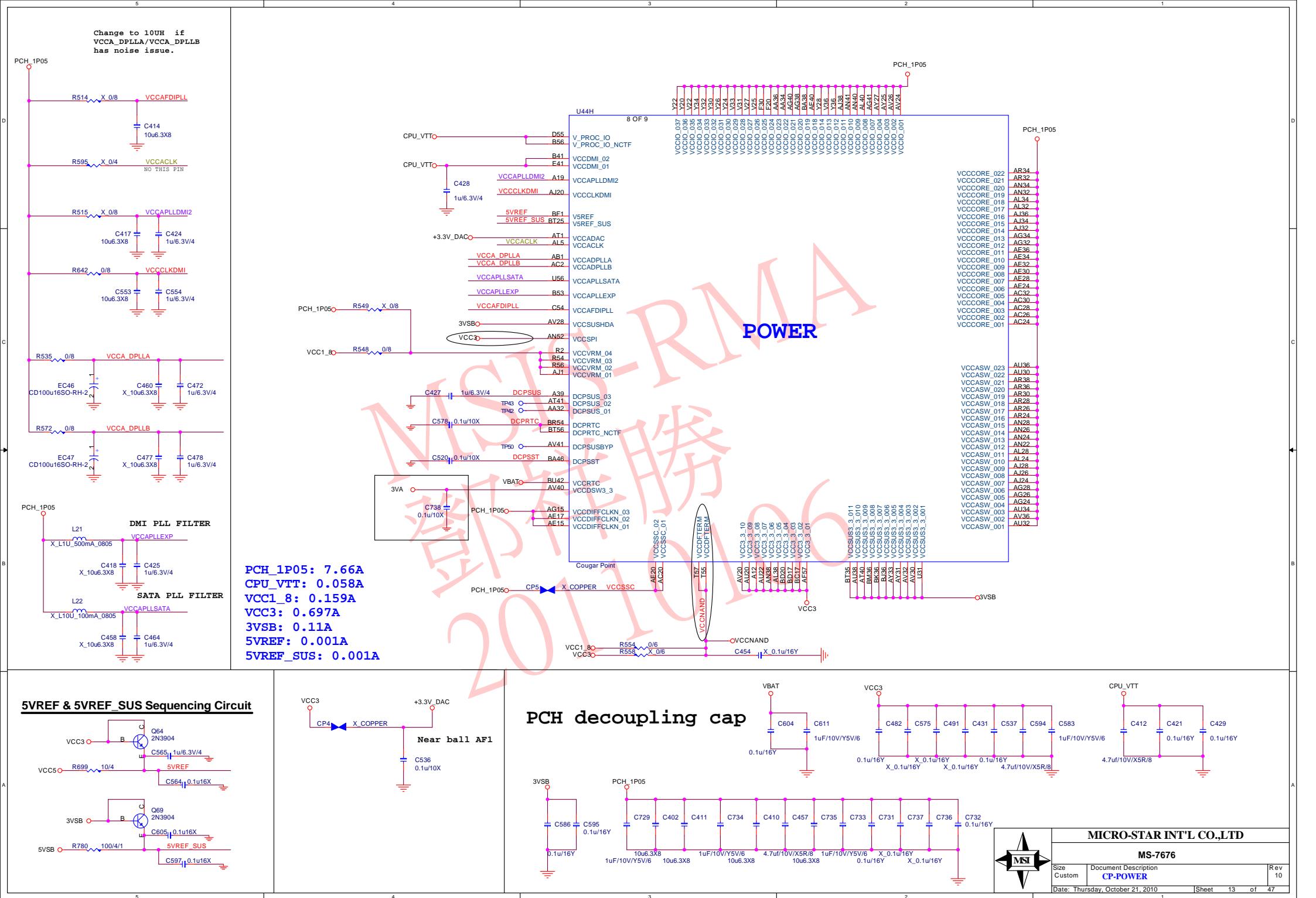
Enable VGA(CTRLCLK/DATA Pull High)

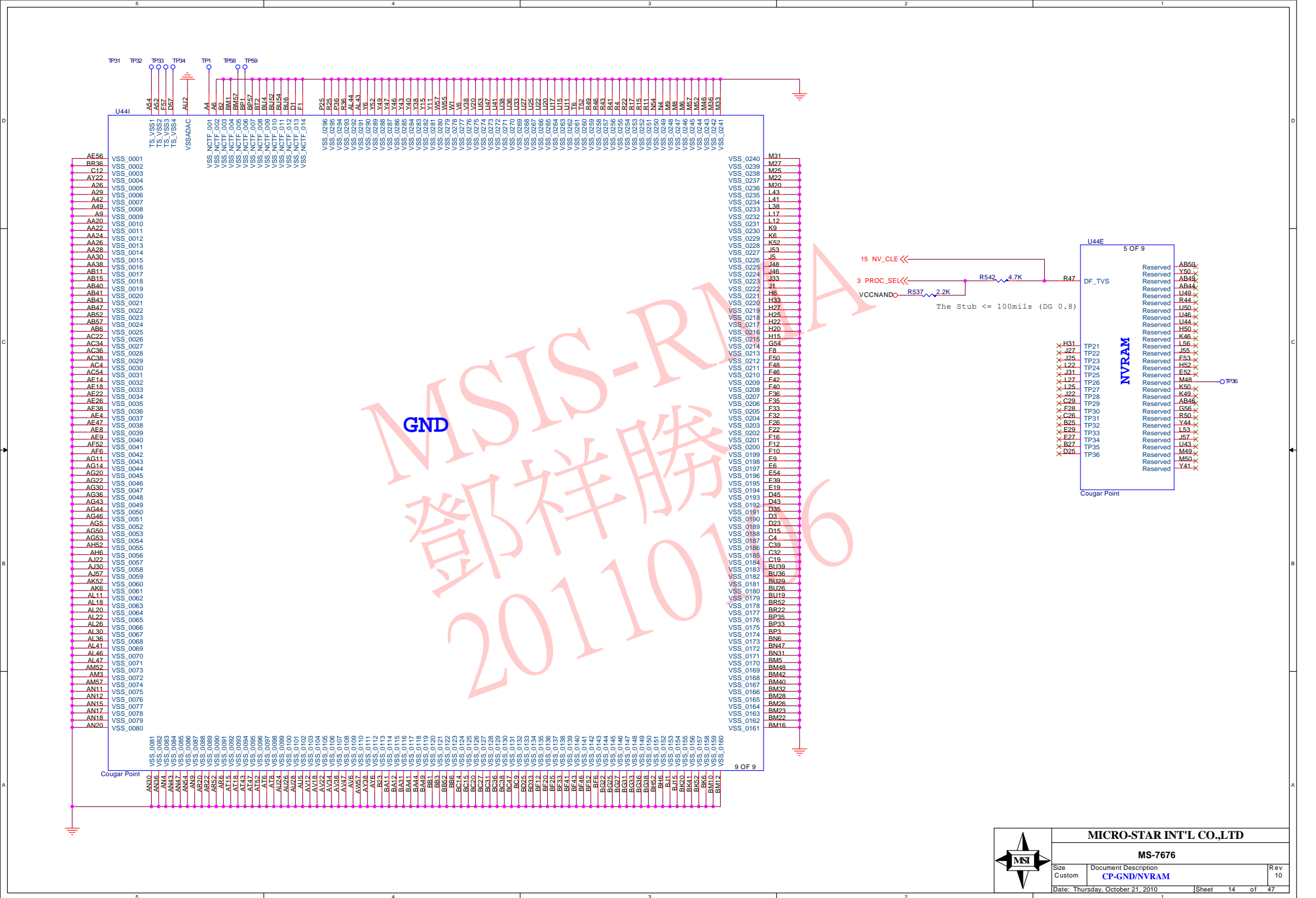


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GND

NVRAM

U44E

DF_TVS

5 OF 9

TP36

Cougar Point



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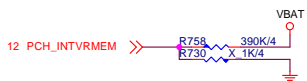
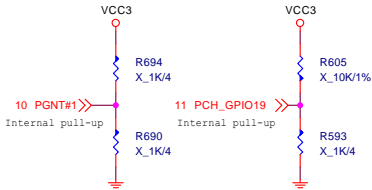
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PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



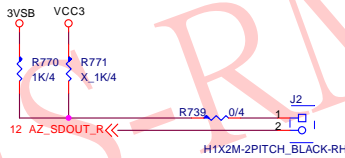
INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltageregulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



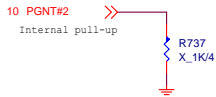
DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.

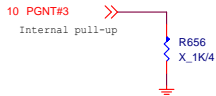


HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

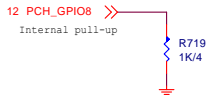
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



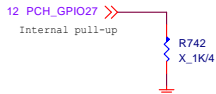
DMI AC/DC MODE
0 : AC
1 : DC *



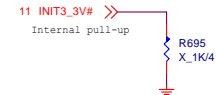
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

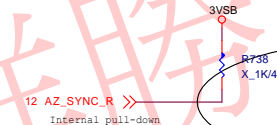


GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INT3_3V#
0 : ??????????????
1 : ?????????????? *

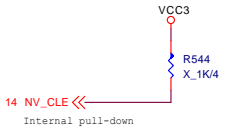
1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



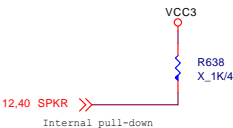
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY




GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

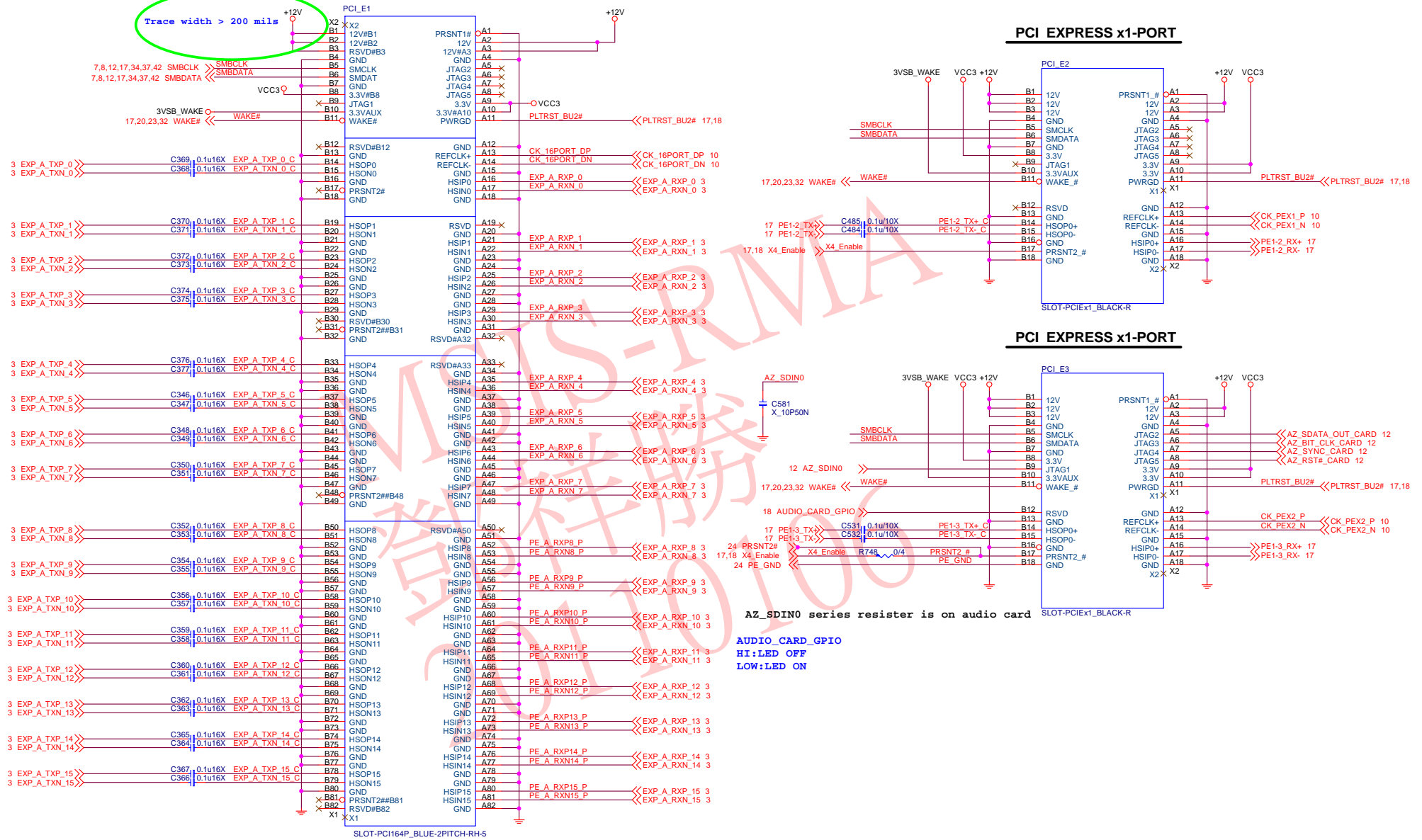


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PCI_Express X16 slot

PCI EXPRESS x1-PORT

PCI EXPRESS x1-PORT

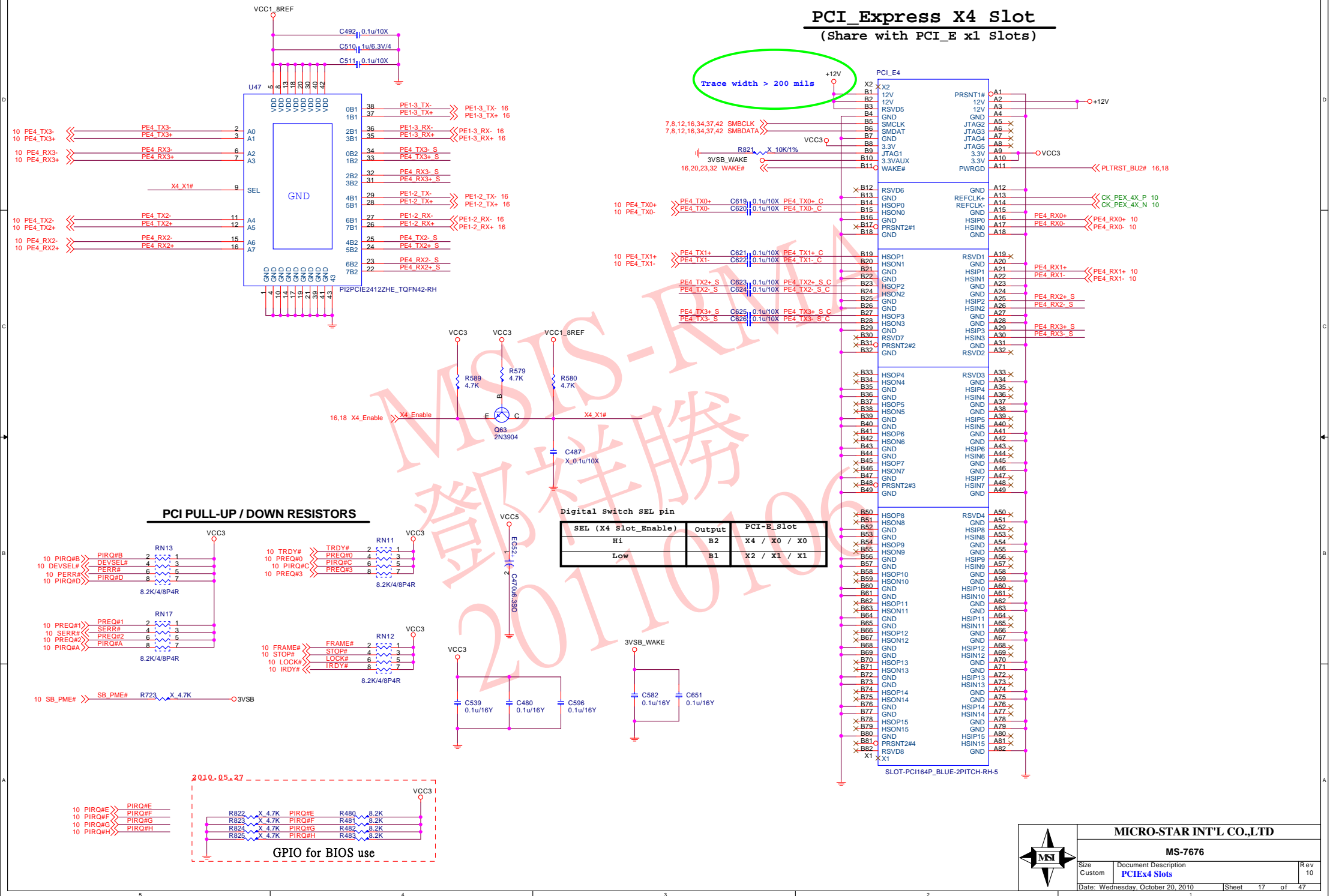


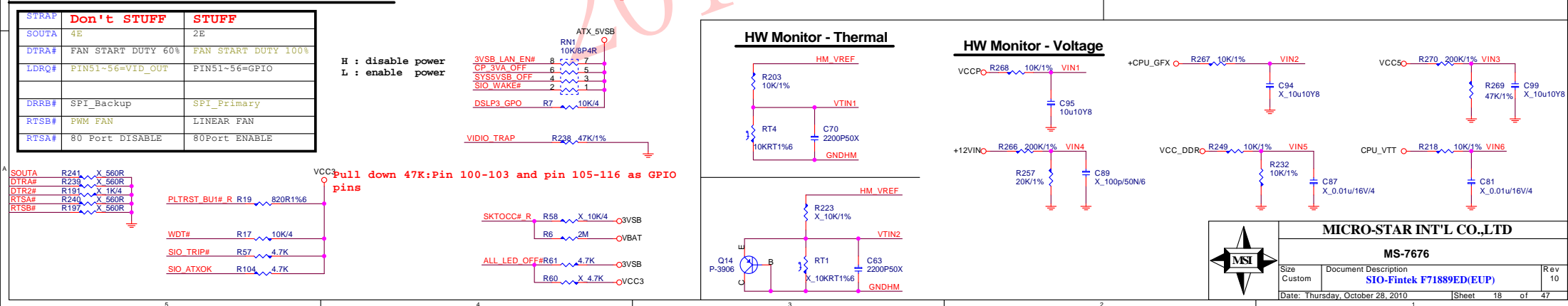
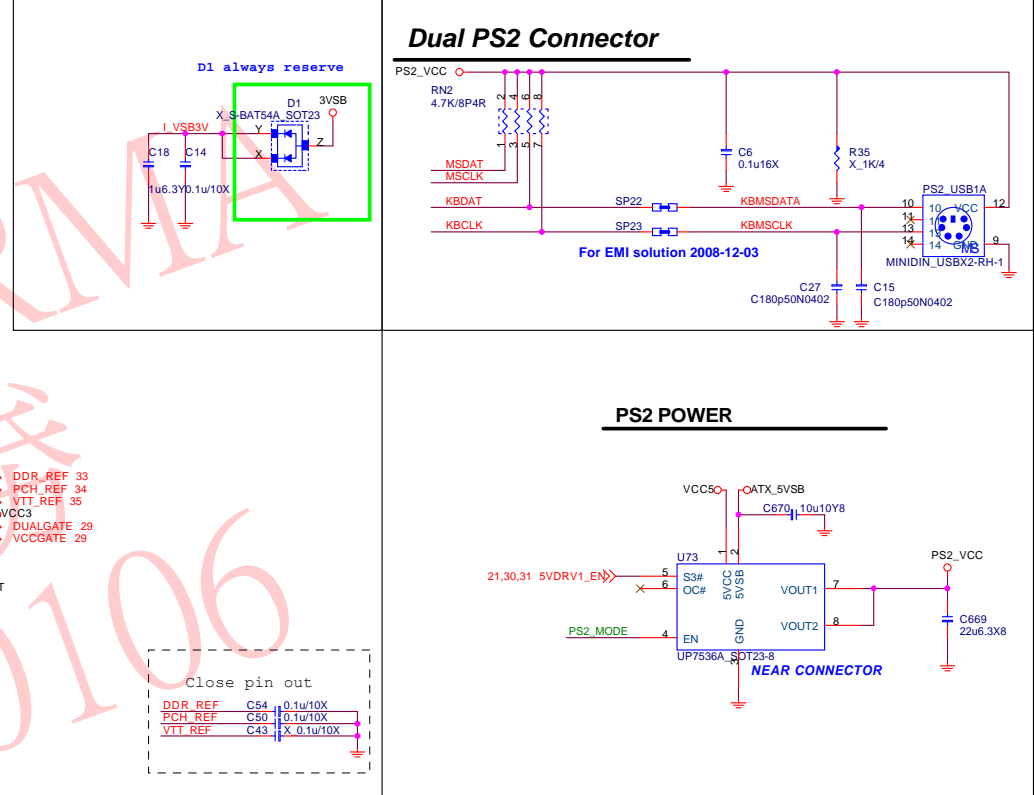
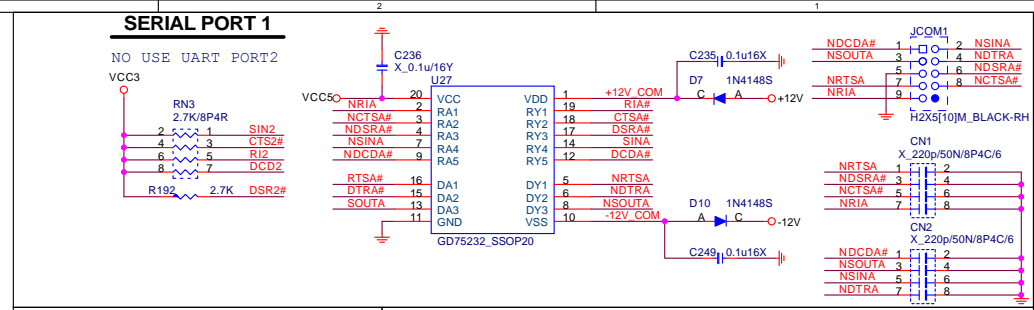
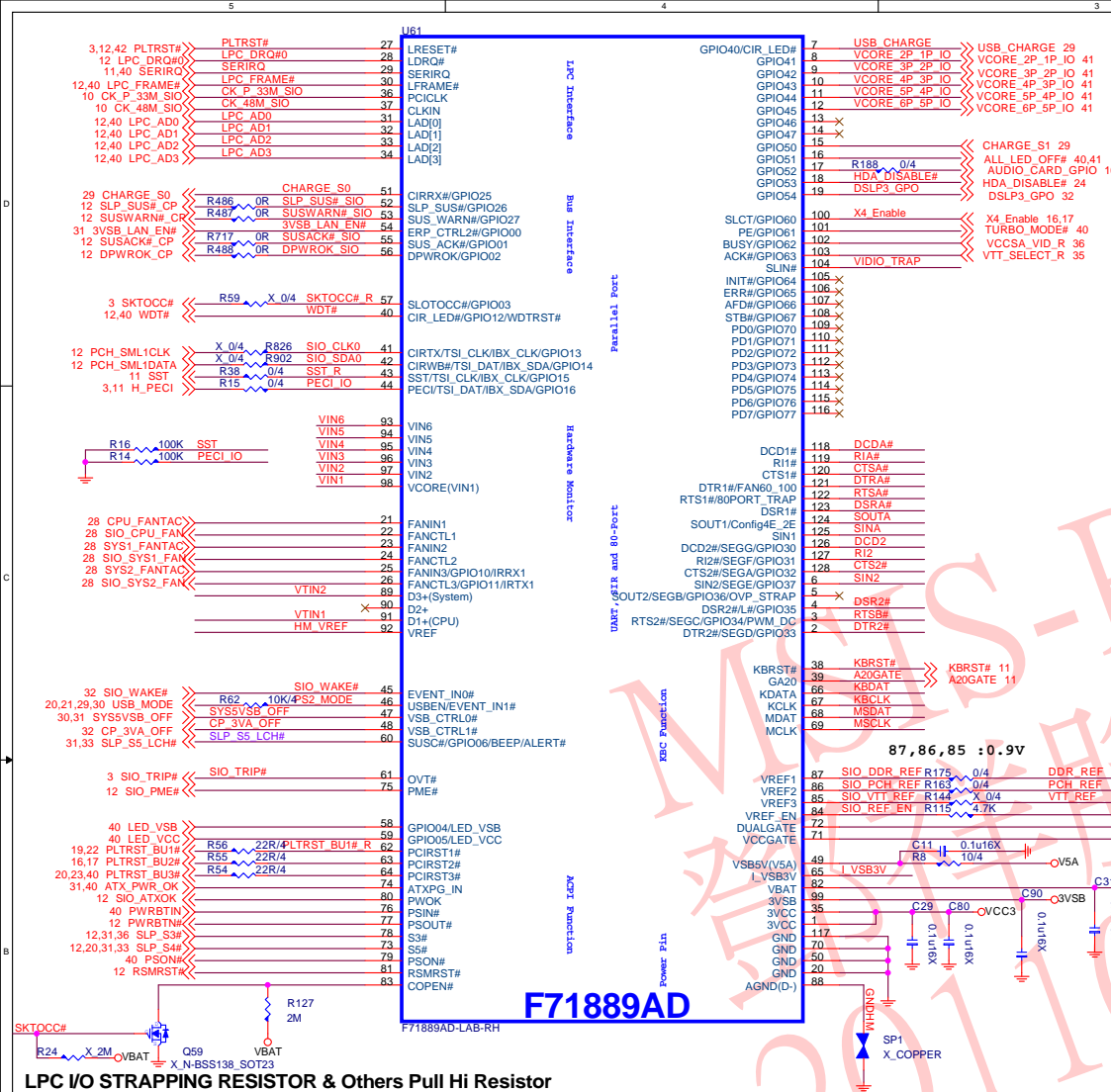
AZ_SDIN0 series resistor is on audio card

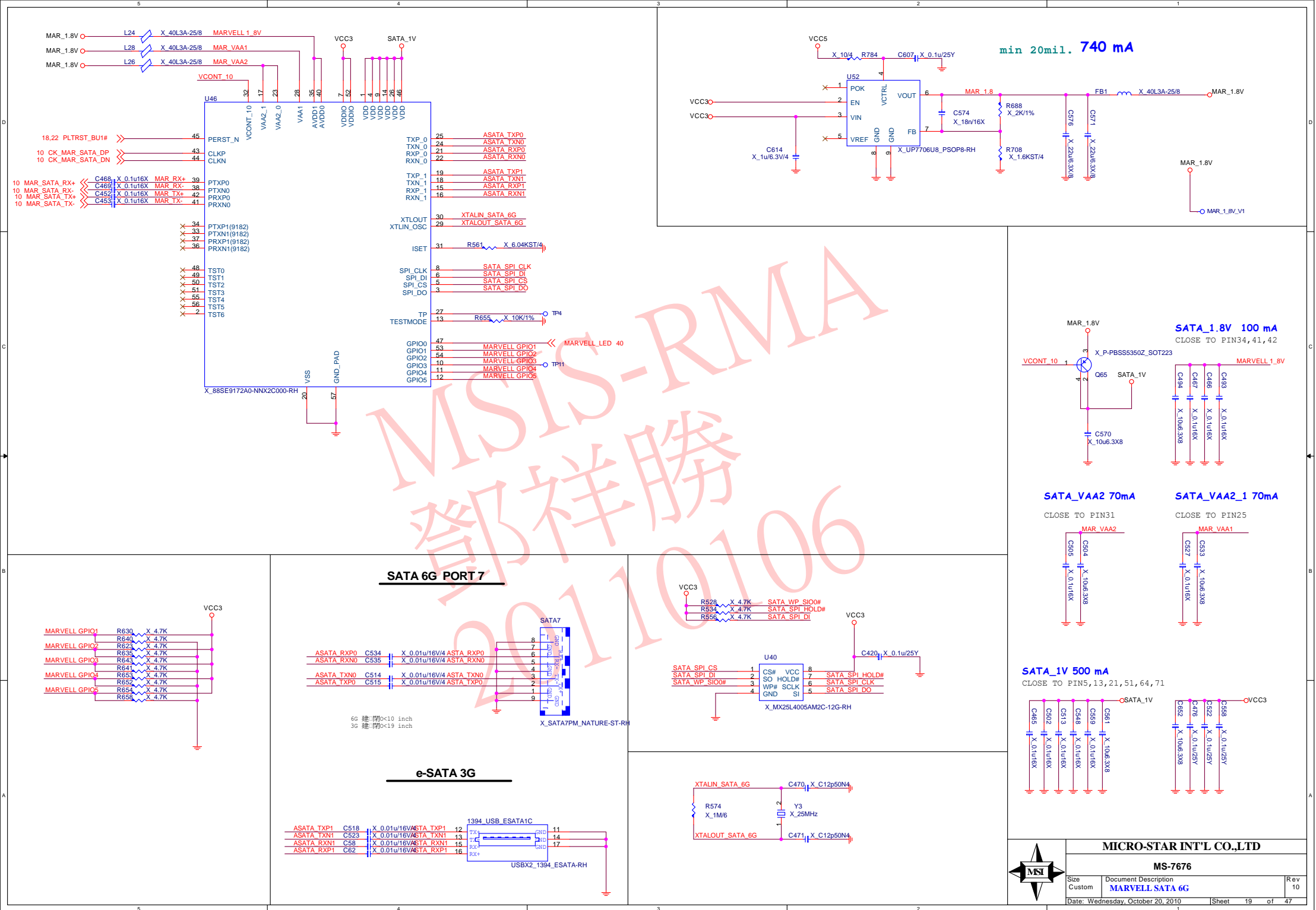
AUDIO_CARD_GPIO
HI:LED OFF
LOW:LED ON

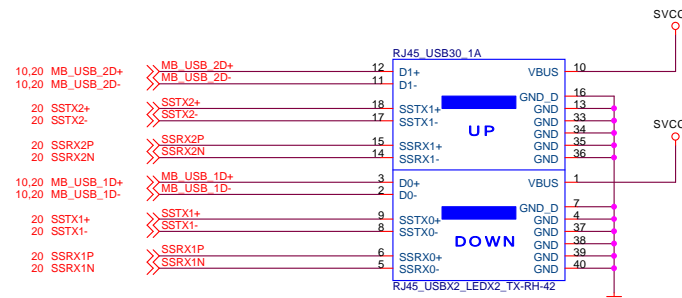
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Custom	PCIE x16 / x1 / x1HDA CO-LAY	10	
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PCI Express X4 Slot (Share with PCI_E x1 Slots)

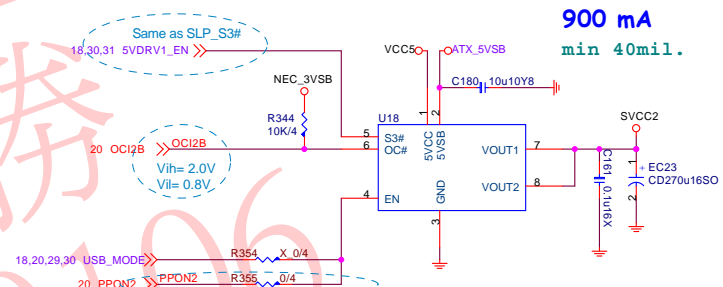
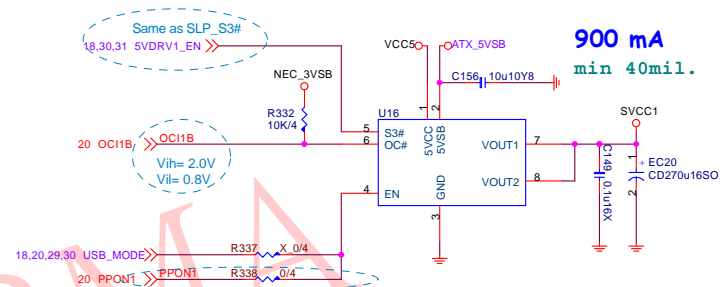








All power sources of uPD720200 are supplied, PPONx is enable.
PPONx is low when OCix going to low.

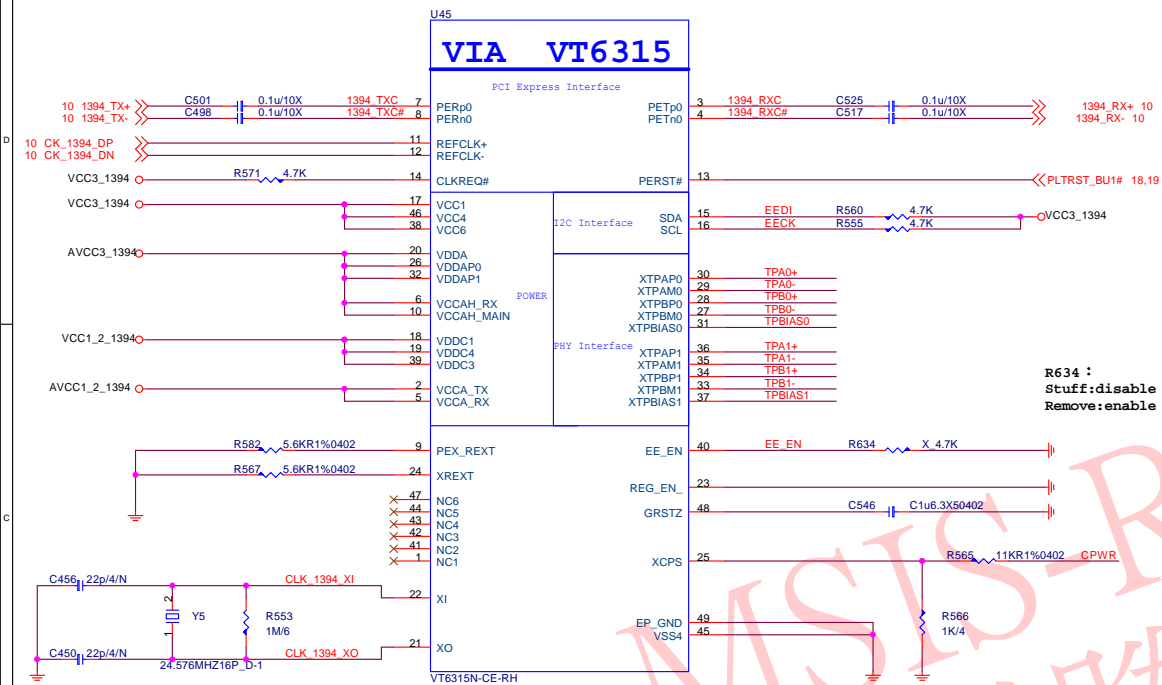


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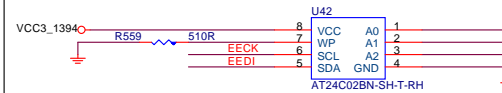
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Custom	NEC USB3.0 POWER & CONNECT	10
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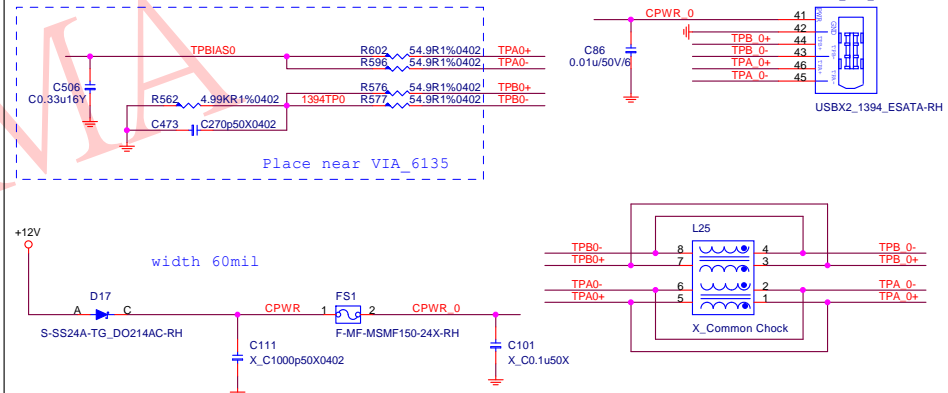
1394 CONTROLLER



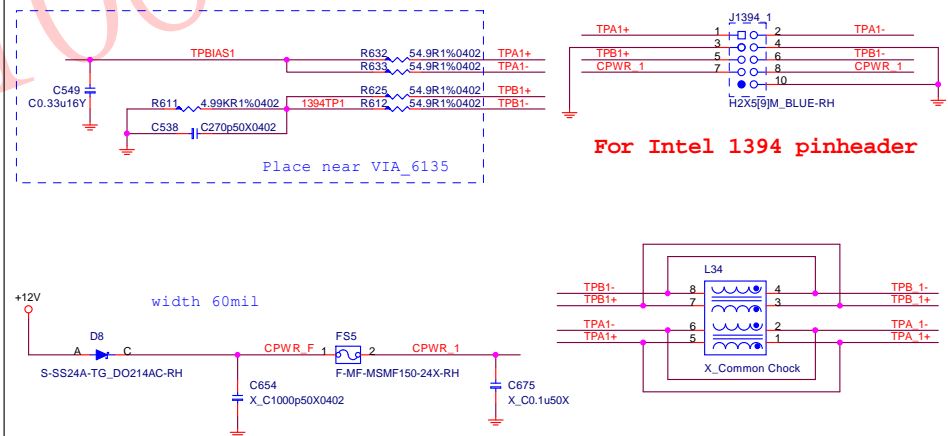
EE PROM



Rear 1394 port



Front 1394 pin header

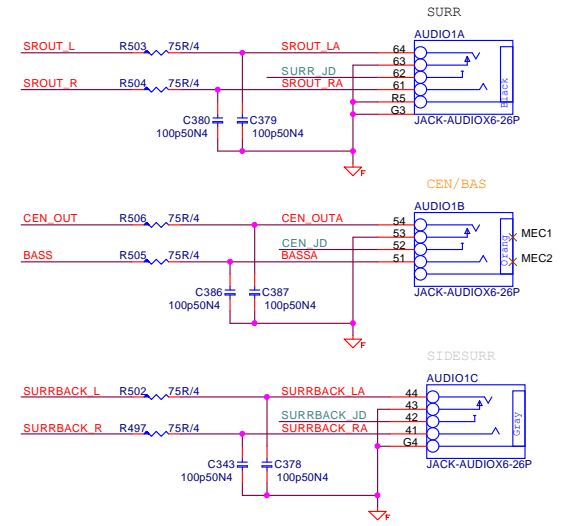


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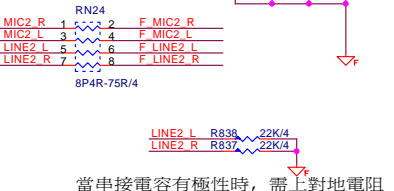
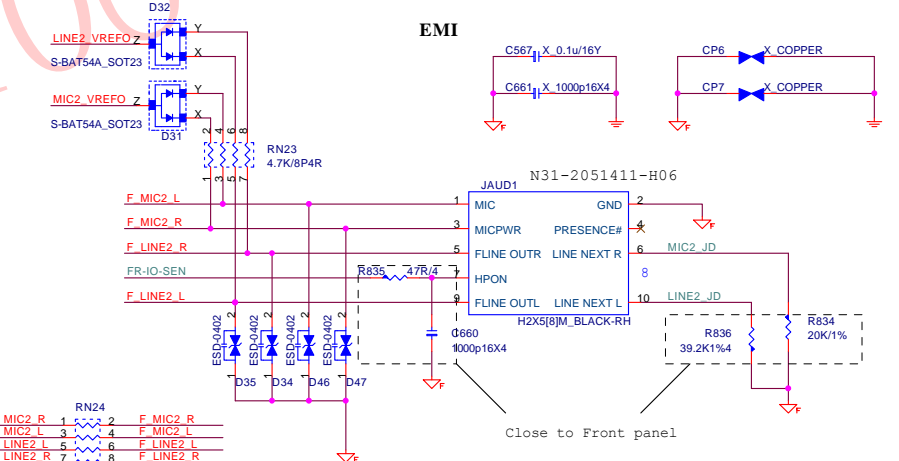
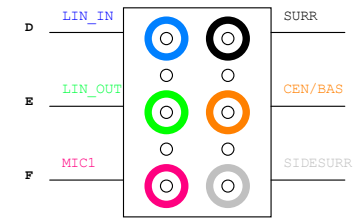
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ALC892

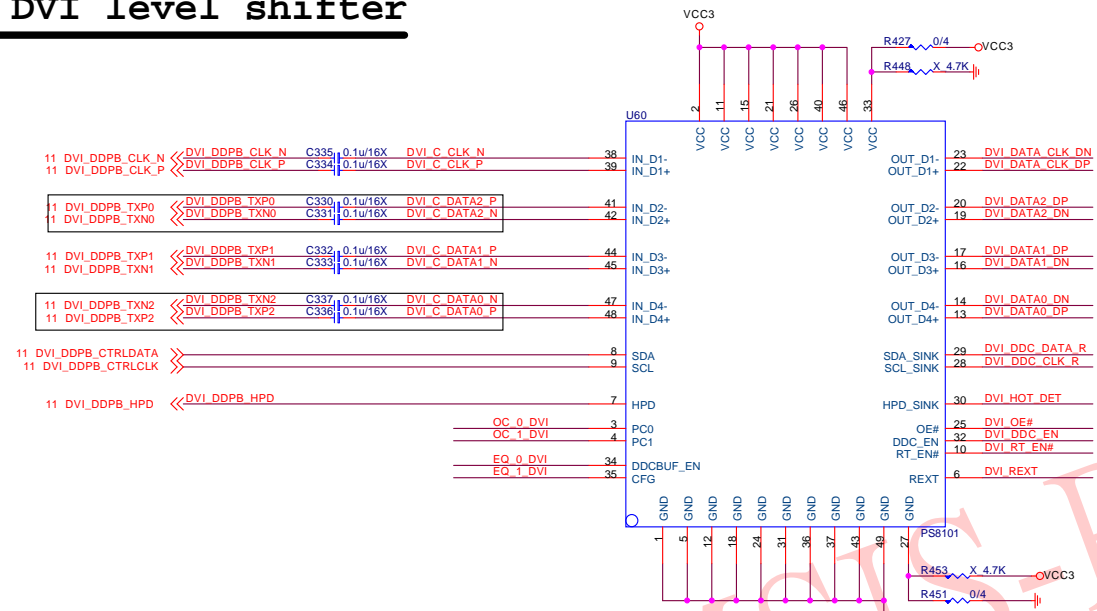


當串接電容有極性時，需上對地電阻



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DVI level shifter

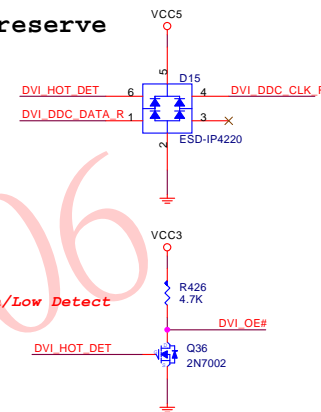


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PARADE料號:B0B-081010C-P97.

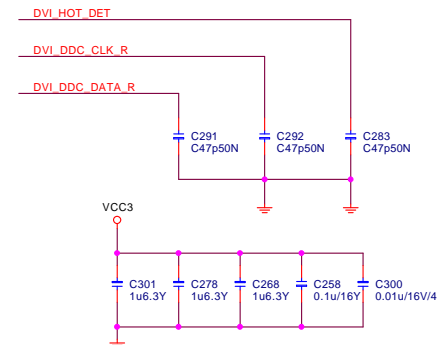
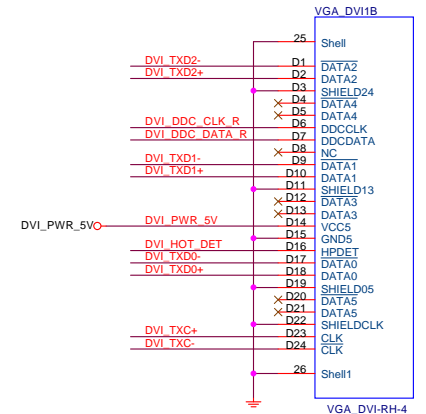
Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_ON
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_OP
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMI_CTRL_DATA	

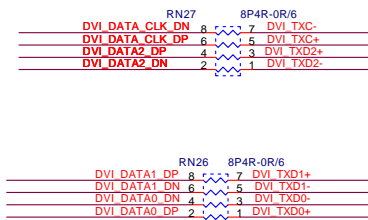
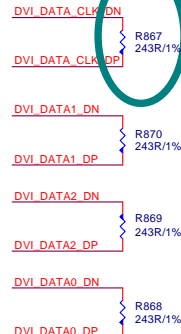
reserve



注 NHigh/Low Detect



EMI



	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

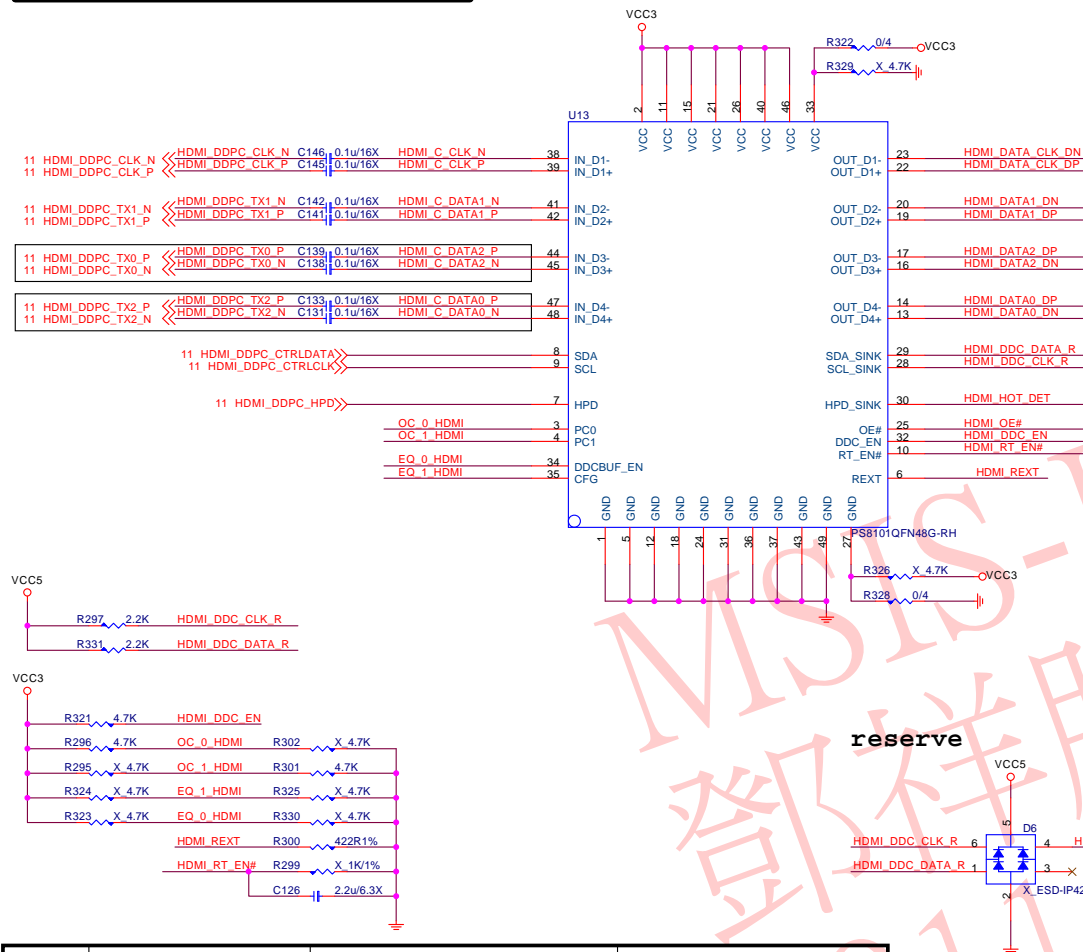
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HDMI level shifter



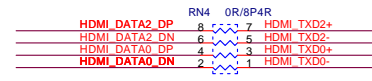
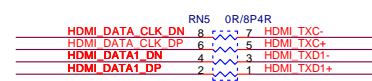
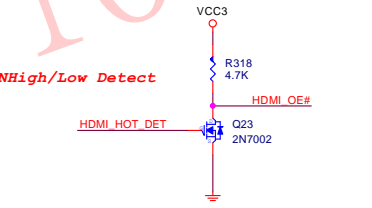
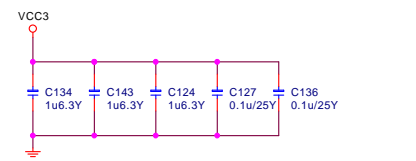
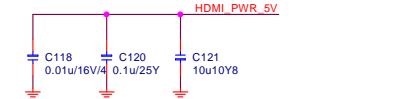
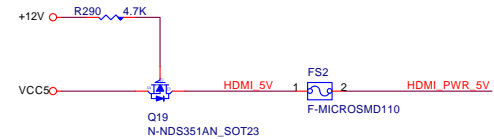
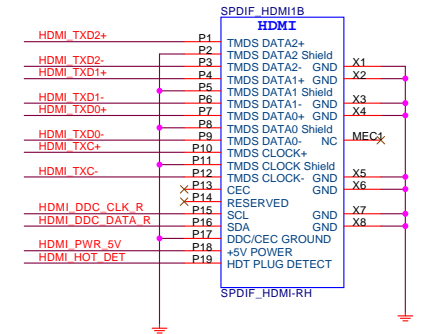
	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.


DDC_EN, DDCBUF_EN, OE#	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_ON
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_OP
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI8_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMI8_CTRL_DATA	





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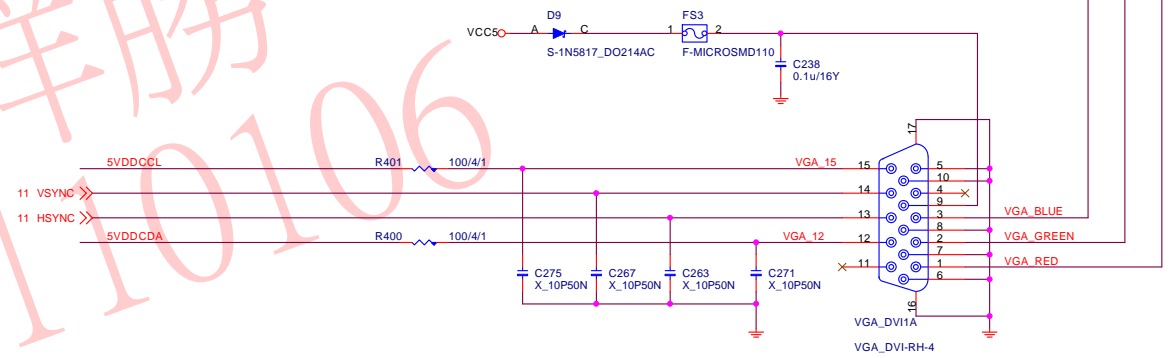
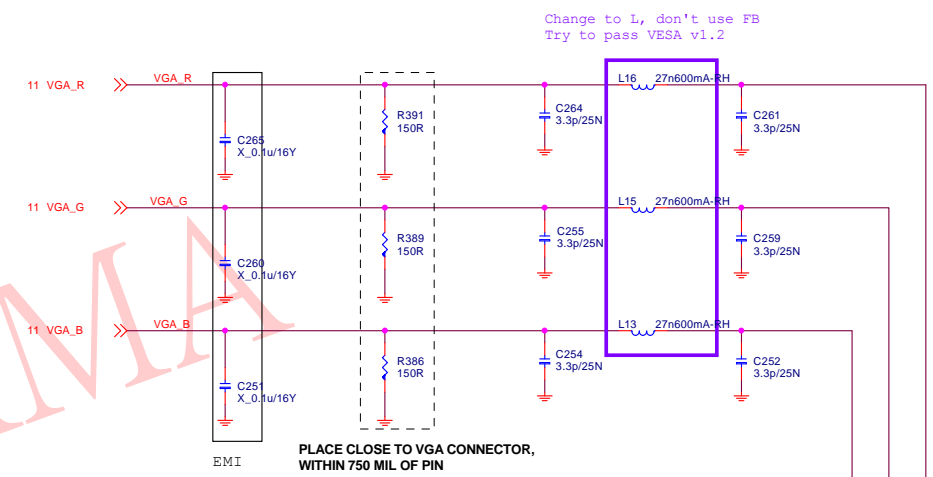
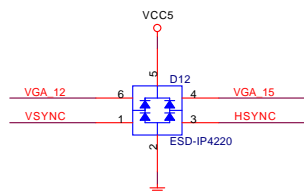
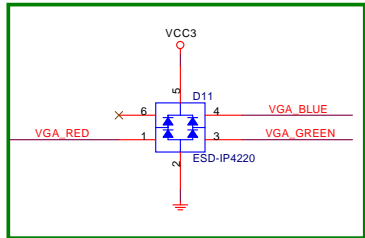
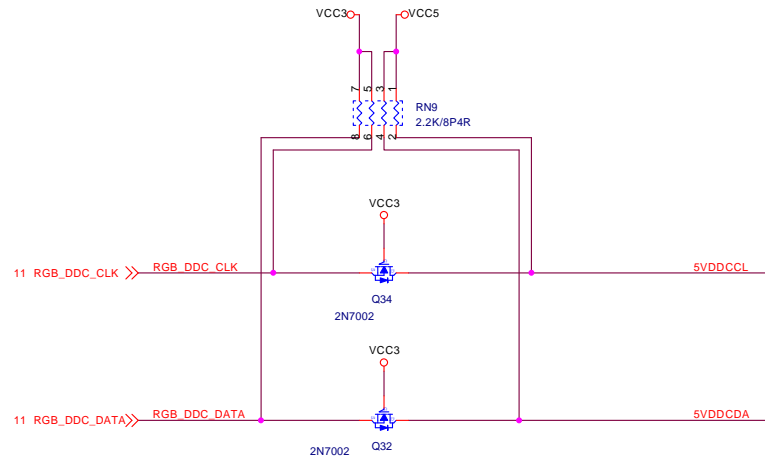
MS-7676

Size Custom Document Description HDMI

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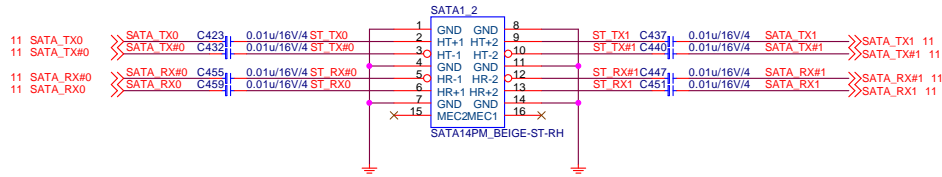
D-Sub

Level shift

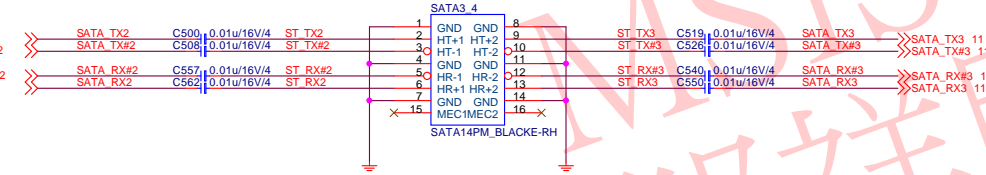


MICRO-STAR INT'L CO.,LTD			
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Size	Document Description		Rev
Custom	VGA		10
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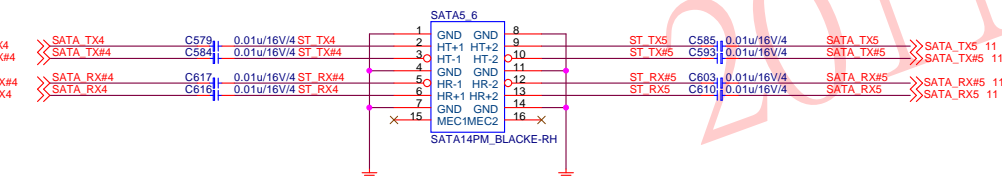
SATA 6G PORT 0,1



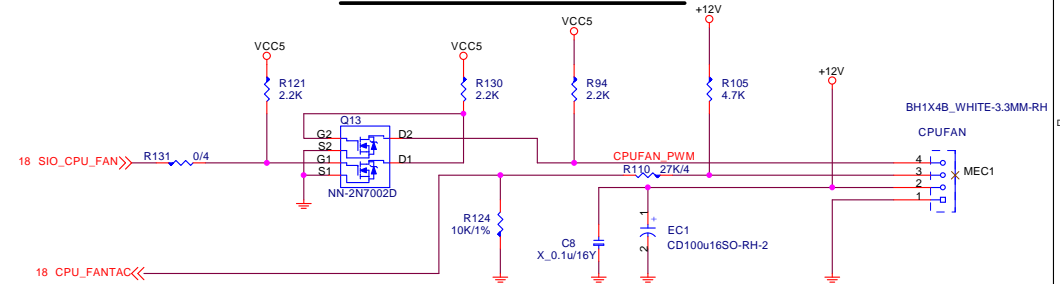
SATA 3G PORT 2,3



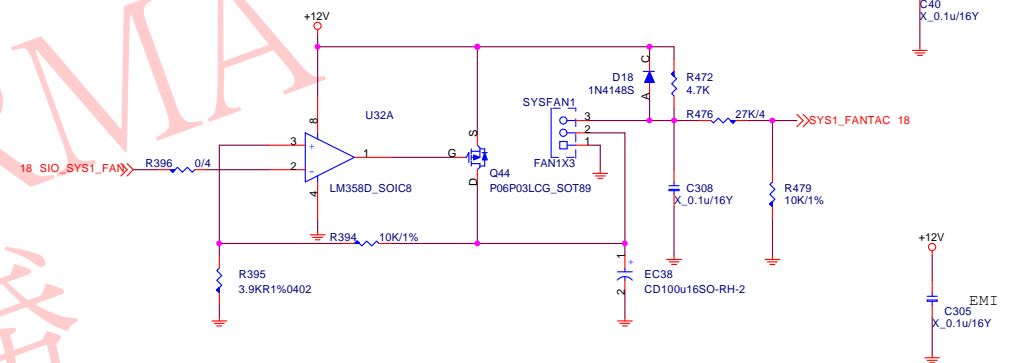
SATA 3G PORT 4,5



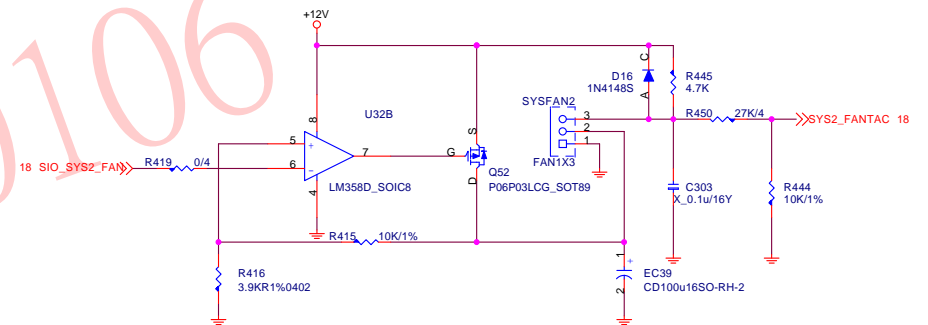
CPU FAN-COUNTROL CIRCUIT



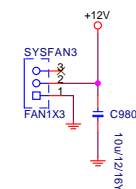
SYSTEM FAN1-COUNTROL CIRCUIT



SYSTEM FAN2-COUNTROL CIRCUIT

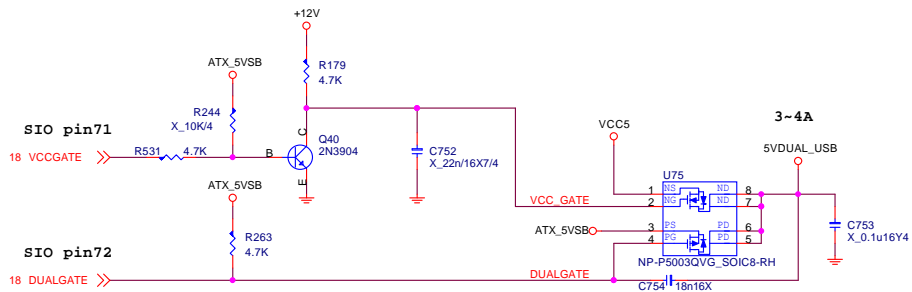


SYSTEM FAN3-12V

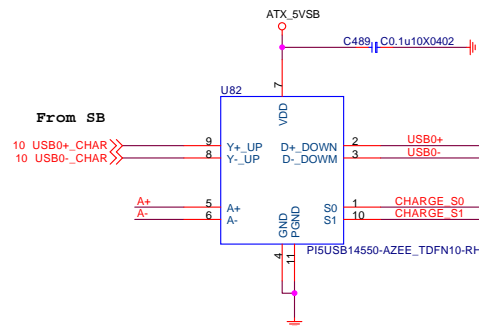
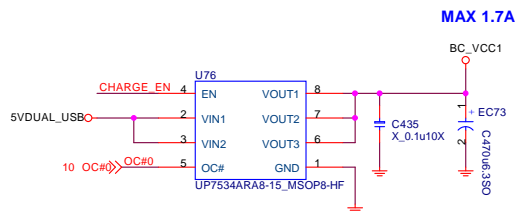


MICRO-STAR INT'L CO.,LTD			
MS-7676			
Size	Custom	Document Description	Rev
		SATA / FAN Control	10
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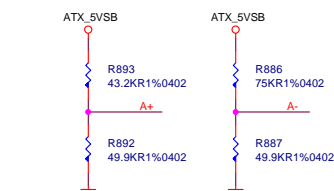
5VDUAL_USB



USB POWER FOR PORT 0 for USBCharging



S1	0	0	1
S0	0	1	1
Mode	AUTO	A	Y



A type
2.70V< D+ <3.1 V,
1.85V< D- < 2.1V*
For i-Pad / i-Phone 4G charges current up to 1.6A.

SIO GPIO40 Pin7 (I_VSB3V)

USB_CHARGE: (OD)
0: Don't support USB charge and resume.
1: Support USB charge and resume.

Power plug in , H/W default support USB charge.

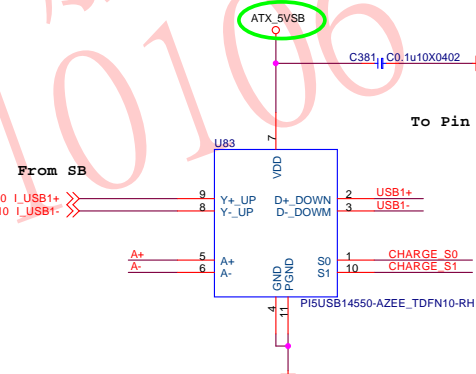
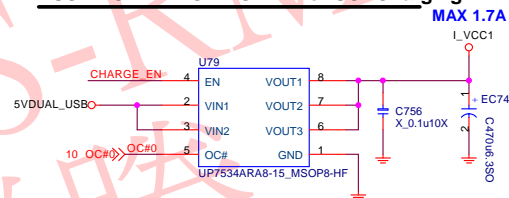
SIO GPIO25 (I_VSB3V)
SIO GPIO50 (I_VSB3V)

CHARGE_S1: (PUSH PULL)
CHARGE_S0: (OPEN DRAIN ONLY)

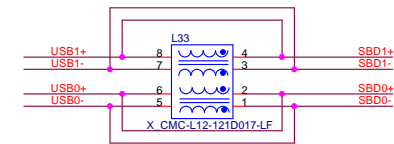
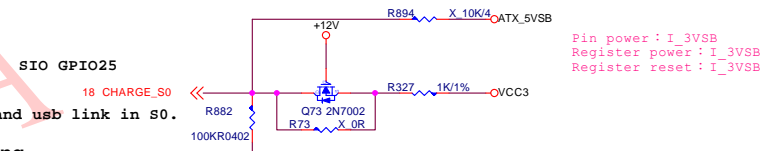
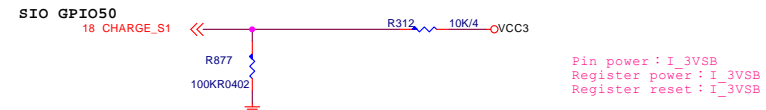
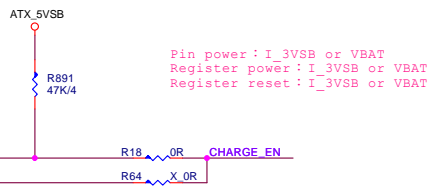
	S0	S1
AUTO:	0	0
DCP :	0	1
A :	1	0
Y :	1	1

H/W default support auto charging in S3/S4/S5 and usb link in S0.

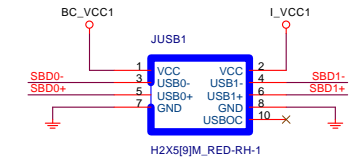
USB POWER FOR PORT 1 for USBCharging



To Pin Header



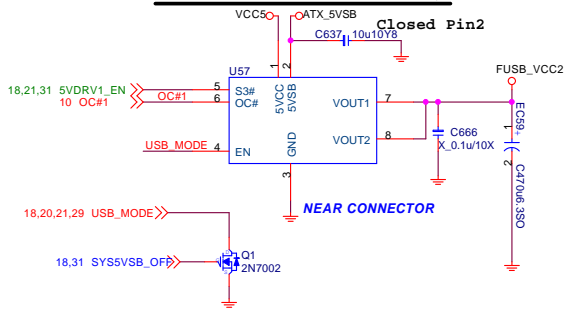
PI5USB14550 has internal EDS diode.



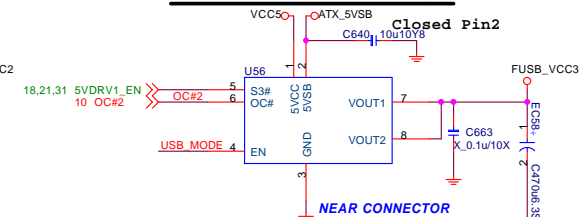
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Front USB Connector

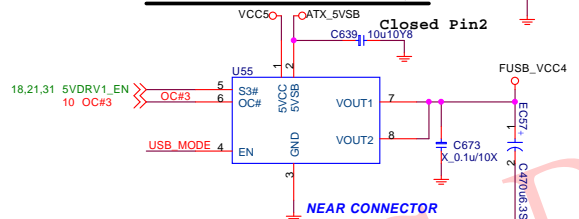
USB POWER REAL PORT 2,3



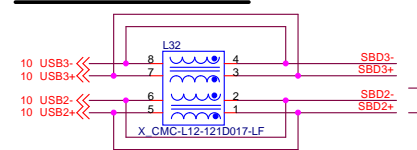
USB POWER FOR PORT 4,5



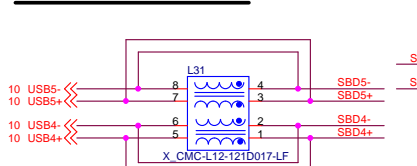
USB POWER FOR PORT 6,7



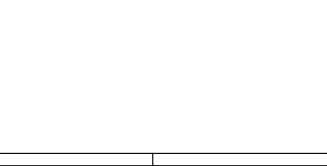
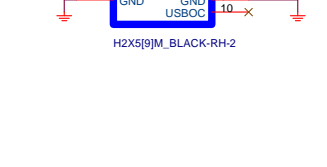
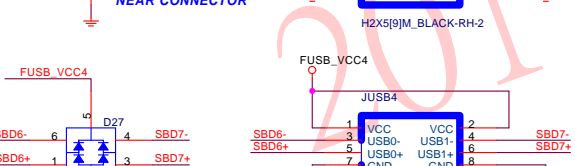
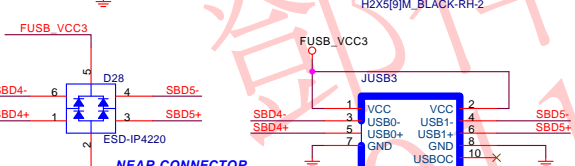
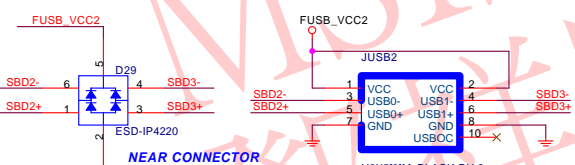
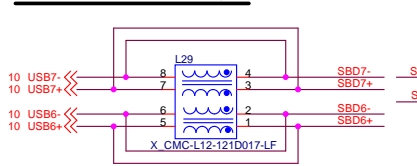
FRONT USB PORT 2,3



FRONT USB PORT 4,5

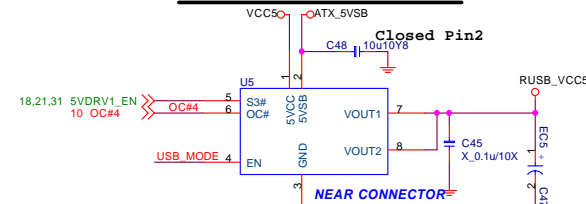


FRONT USB PORT 6,7

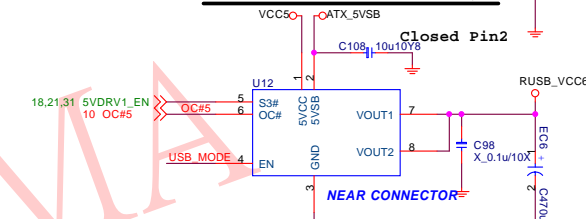


Rear USB Connector

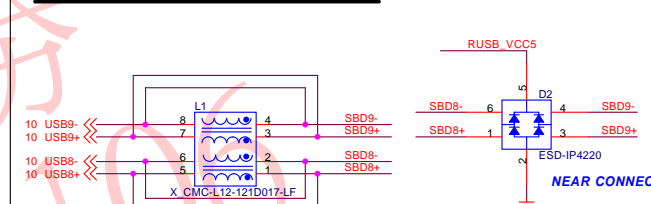
USB POWER FOR PORT 6,7



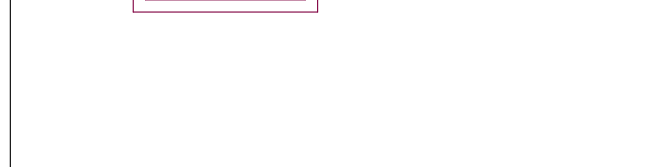
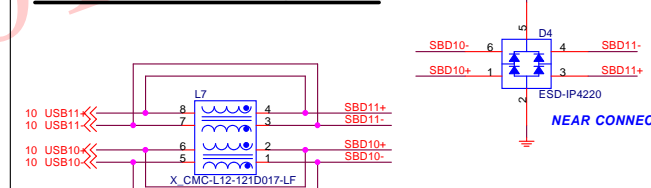
USB POWER FOR PORT 8,9



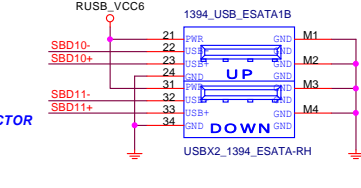
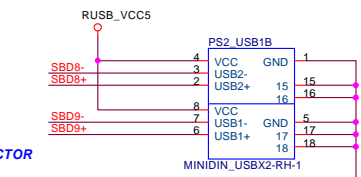
REAR USB PORT 8,9 (With PS2)



REAR USB PORT 10,11 (With 1394)



USB_MODE for USB voltage
H:Follow 5VSB
L:Always off

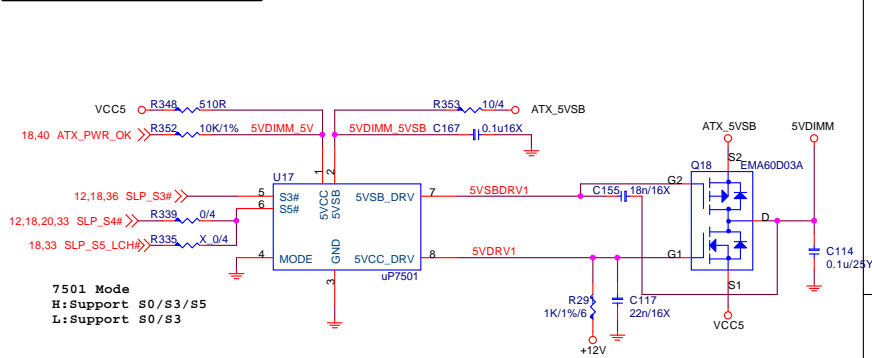


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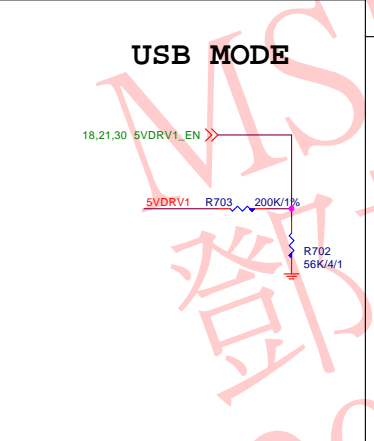
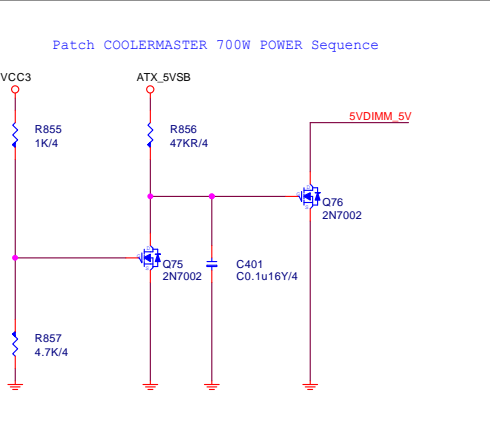
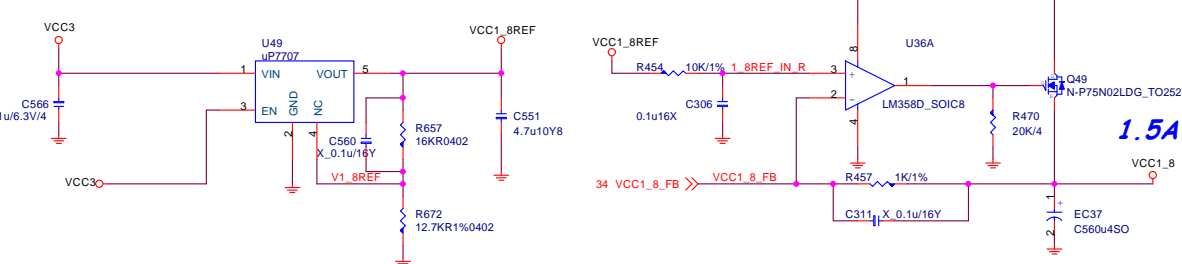
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Custom	USB Connector	10
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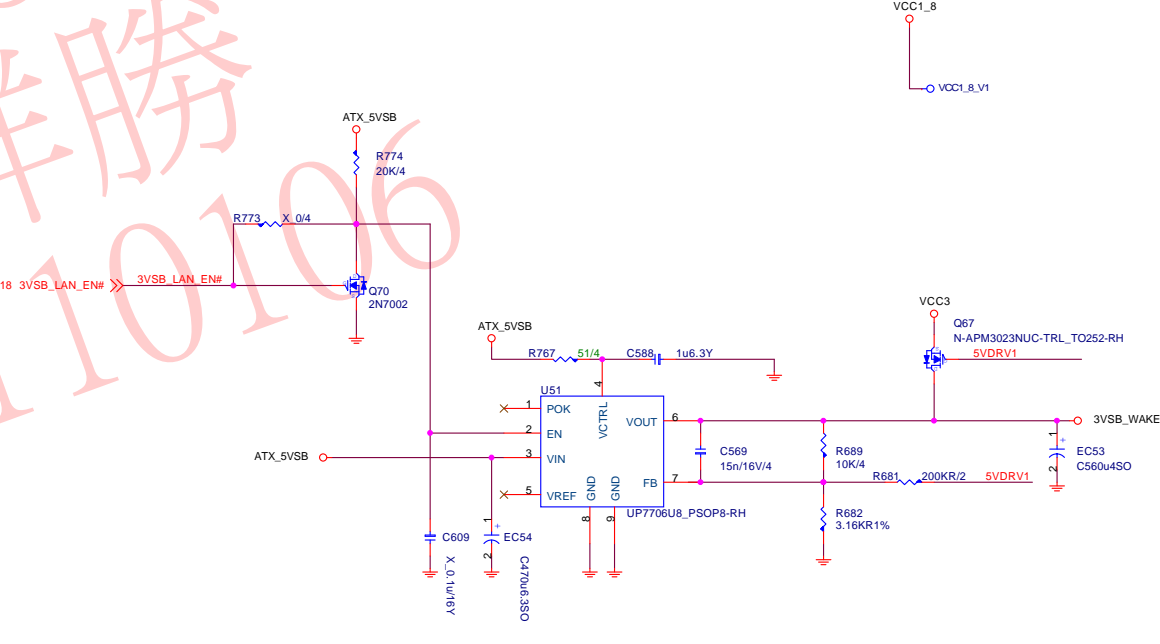
5VDIMM FOR DDR



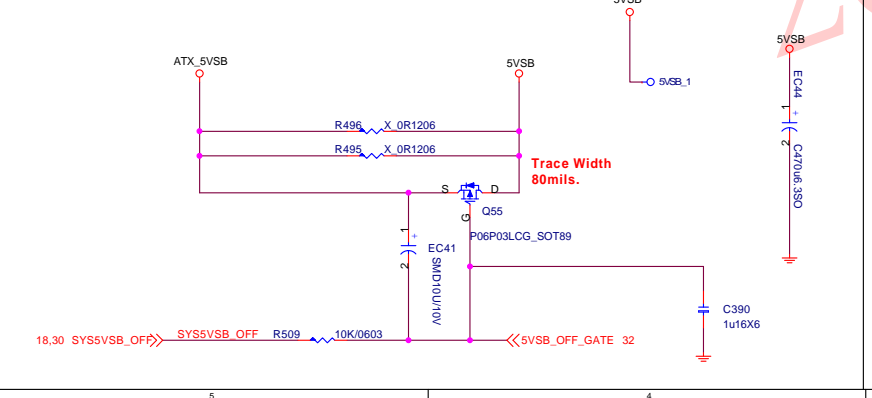
VCC1_8REF



3VSB_WAKE

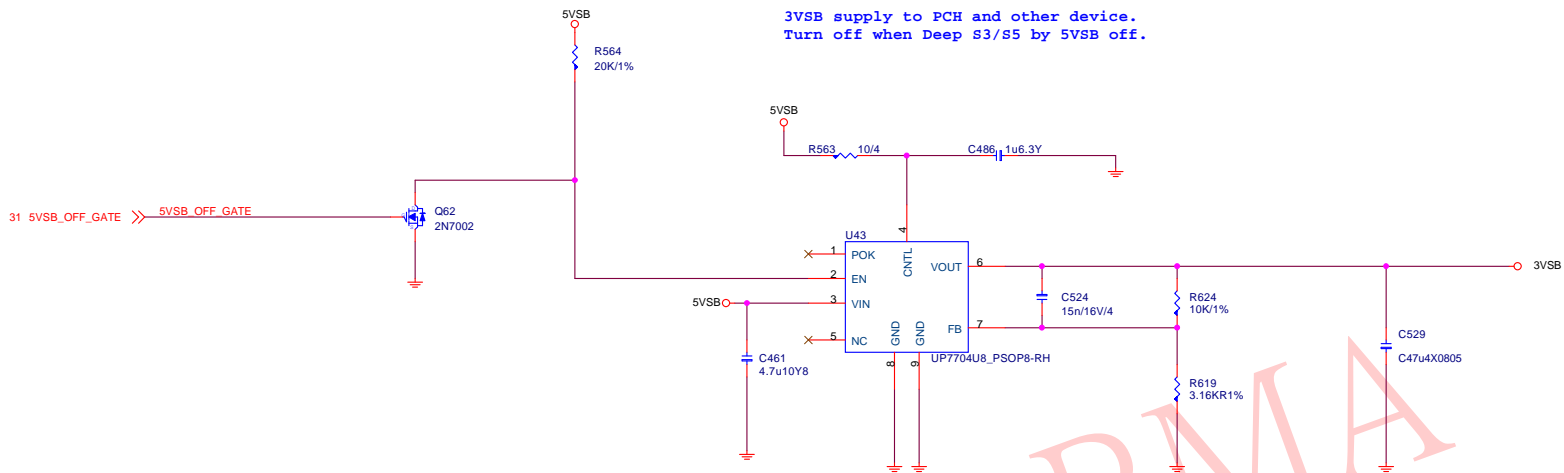


5VSB Power Switch

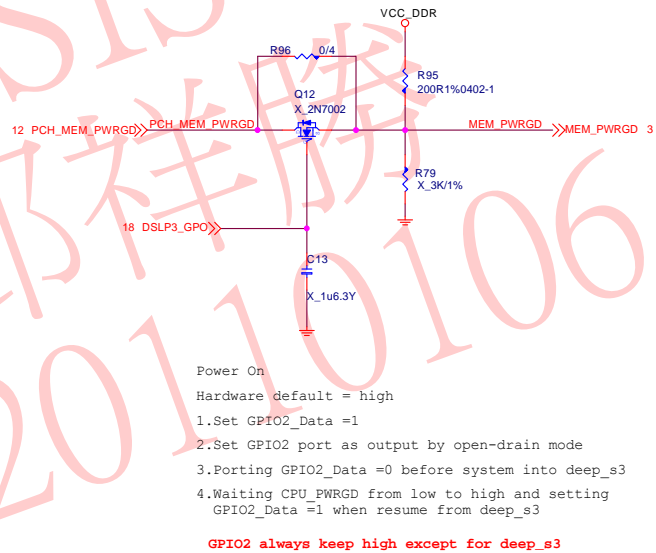
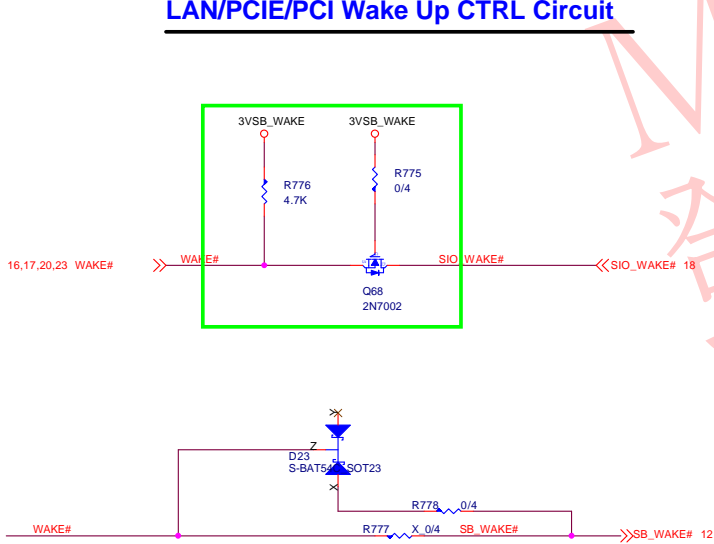


MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size Custom	Document Description ACPI controller UPI	Rev 10
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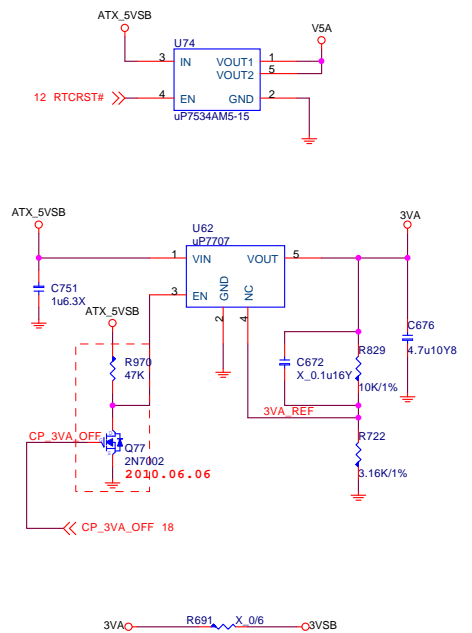
Deep Mode WOL LAN Power CTRL Circuit



LAN/PCIE/PCI Wake Up CTRL Circuit



RTC RST patch circuit for clr-CMOS PCH will wake up issue



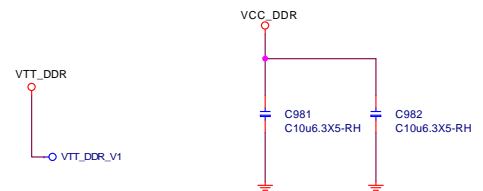
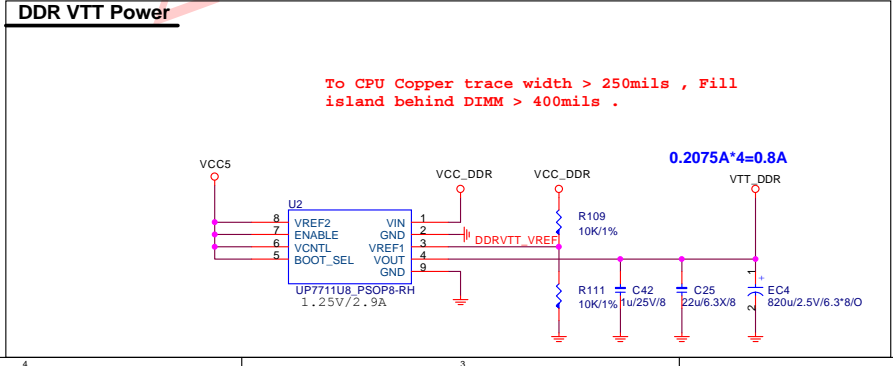
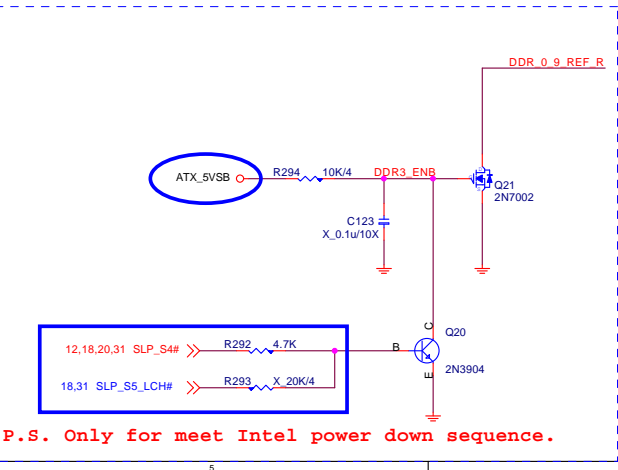
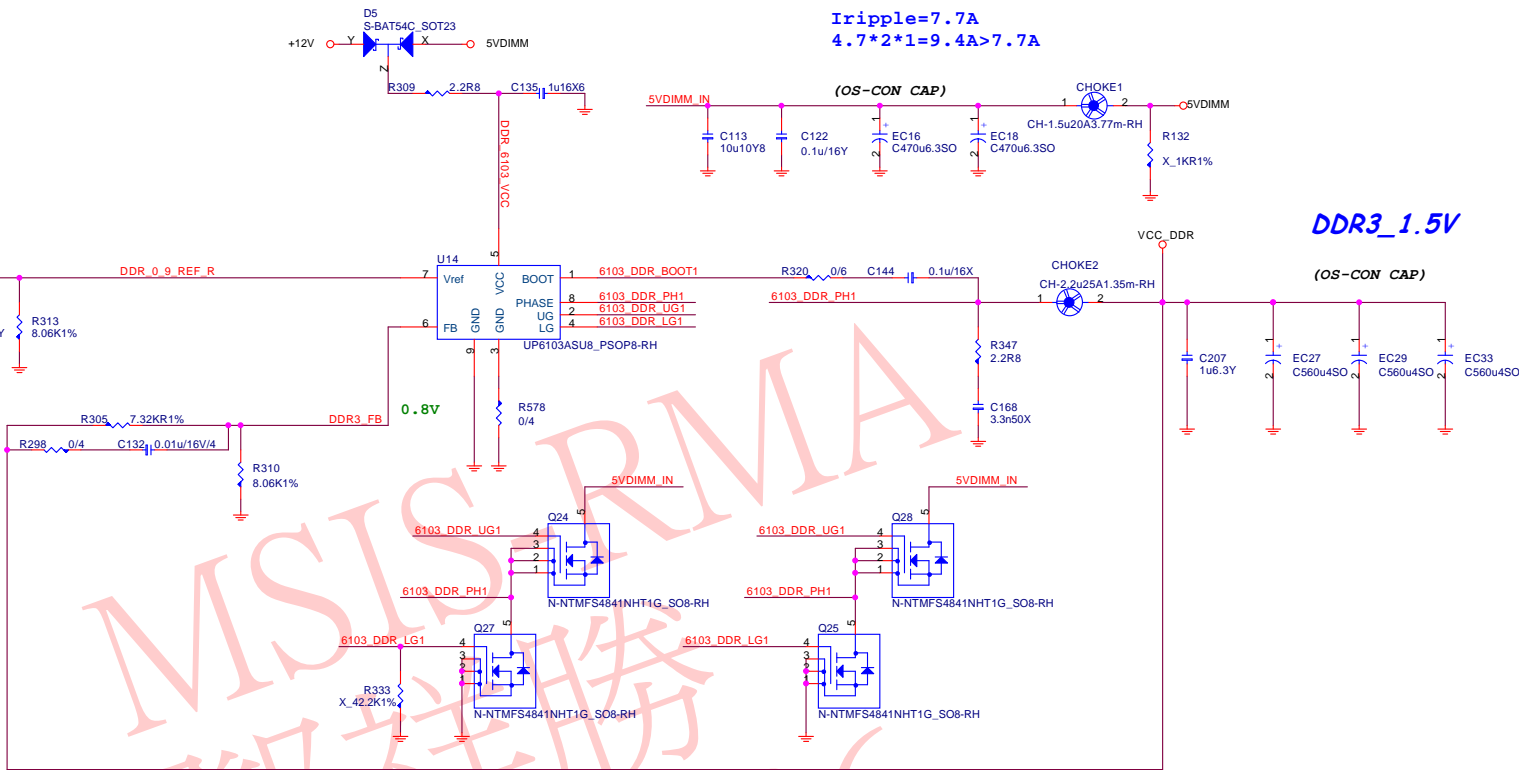
DDR Power:1.5V

DDR3_1.5V 4.5A+15A+1A=20.5A

4.5A FOR CPU
15A FOR 4DIMM
1A FOR DDR VTT

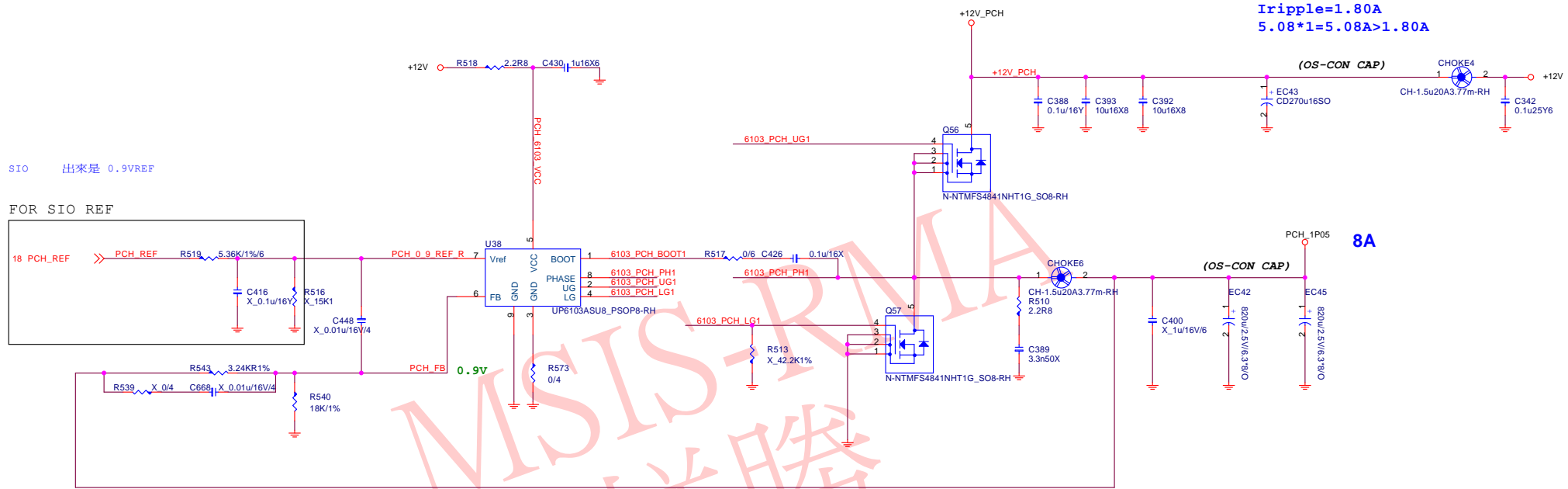
SIO 出來是 0.9VREF

$$(0.9V \times 8.06K) / (1K + 8.06K) = 0.795V$$
$$0.795V (1 + 7.15K / 8.06K) = 1.5V (VCC_DDR)$$



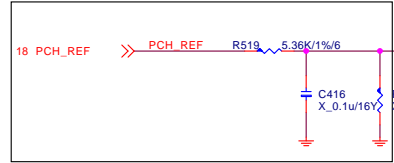
MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size Custom	Document Description DDR Power - uP6103 1-Phase	Rev 10
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PCH Power:1.05V
PCH Core 6.2A+1.8A=8A
6.2A FOR PCH
1.8A FOR ME CORE

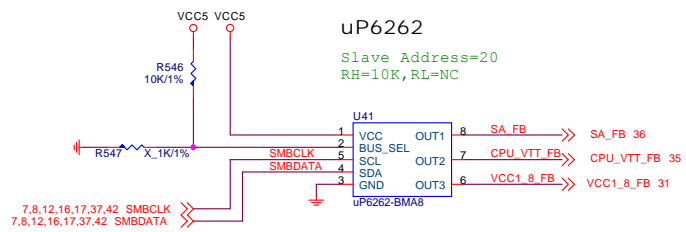
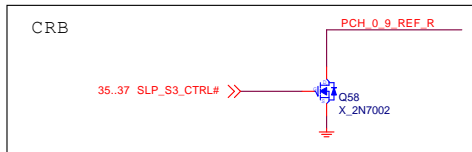


SIO 出來是 0.9VREF

FOR SIO REF



UPI VOLTAGE CONSOLE

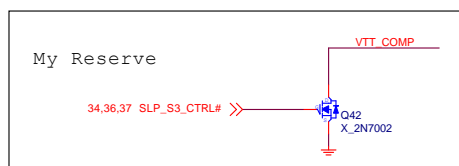
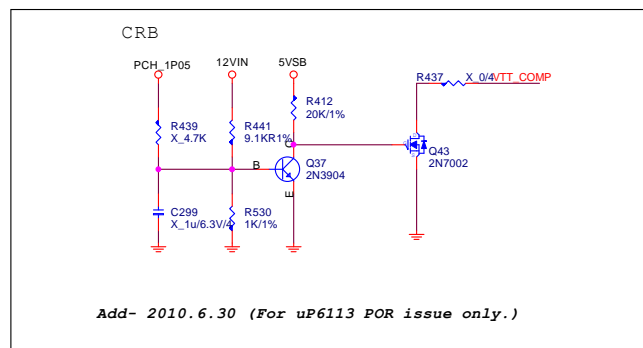


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Size	Document Description	Rev	
Custom	PCH Power - uP6103 1-Phase	10	
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CPU_VTT:1.05/1.00

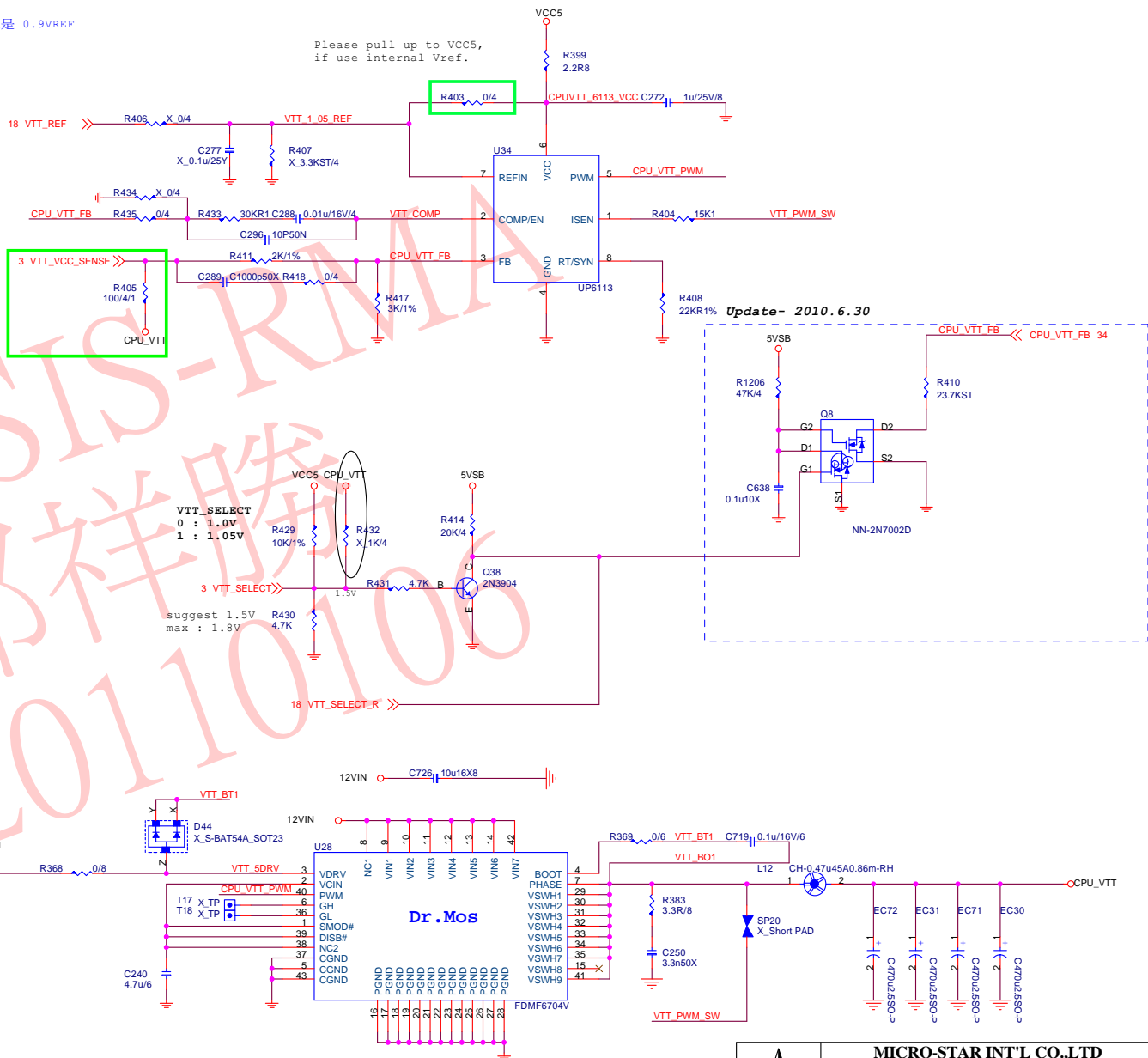
CPU VTT 8.5A

8.5A FOR CPU



SIO 出來是 0.9VREF

Please pull up to VCC5,
if use internal Vref.

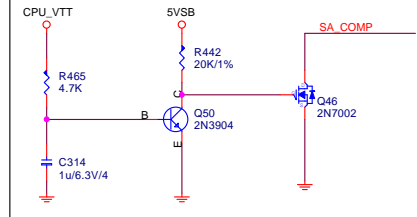


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Size	Document Description	Rev
Custom	CPU_VTT - uP6113- 1-Phase	10
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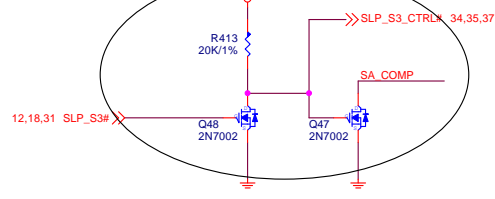
CPU_SA:0.925/0.85

SA Core =8.8A

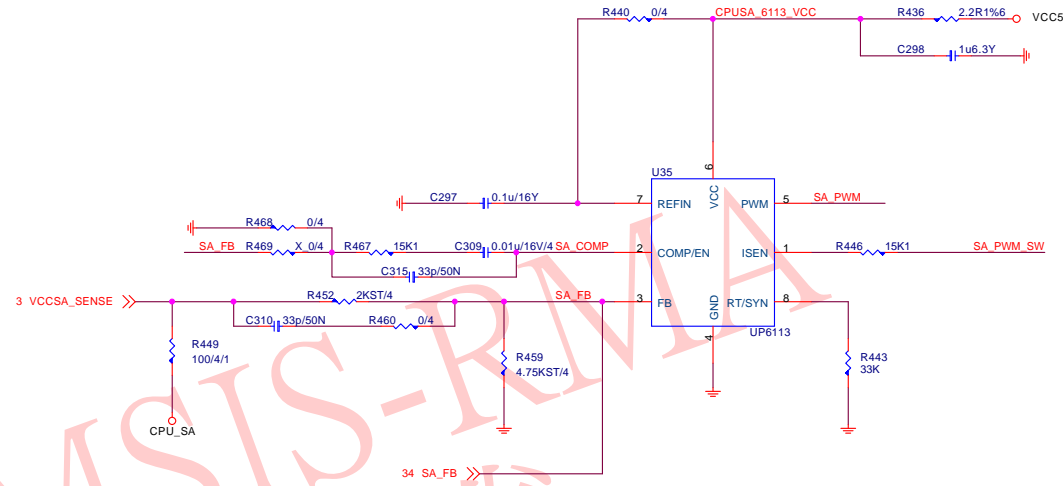
Waitting CPU_VTT Ready



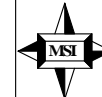
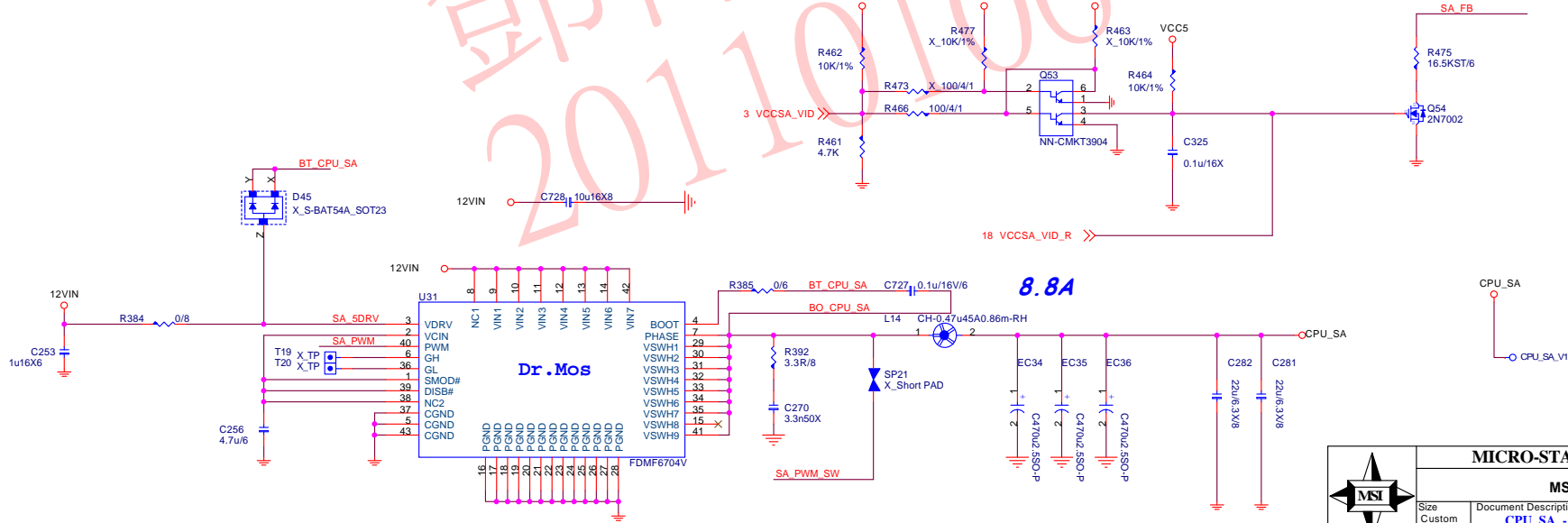
CRB



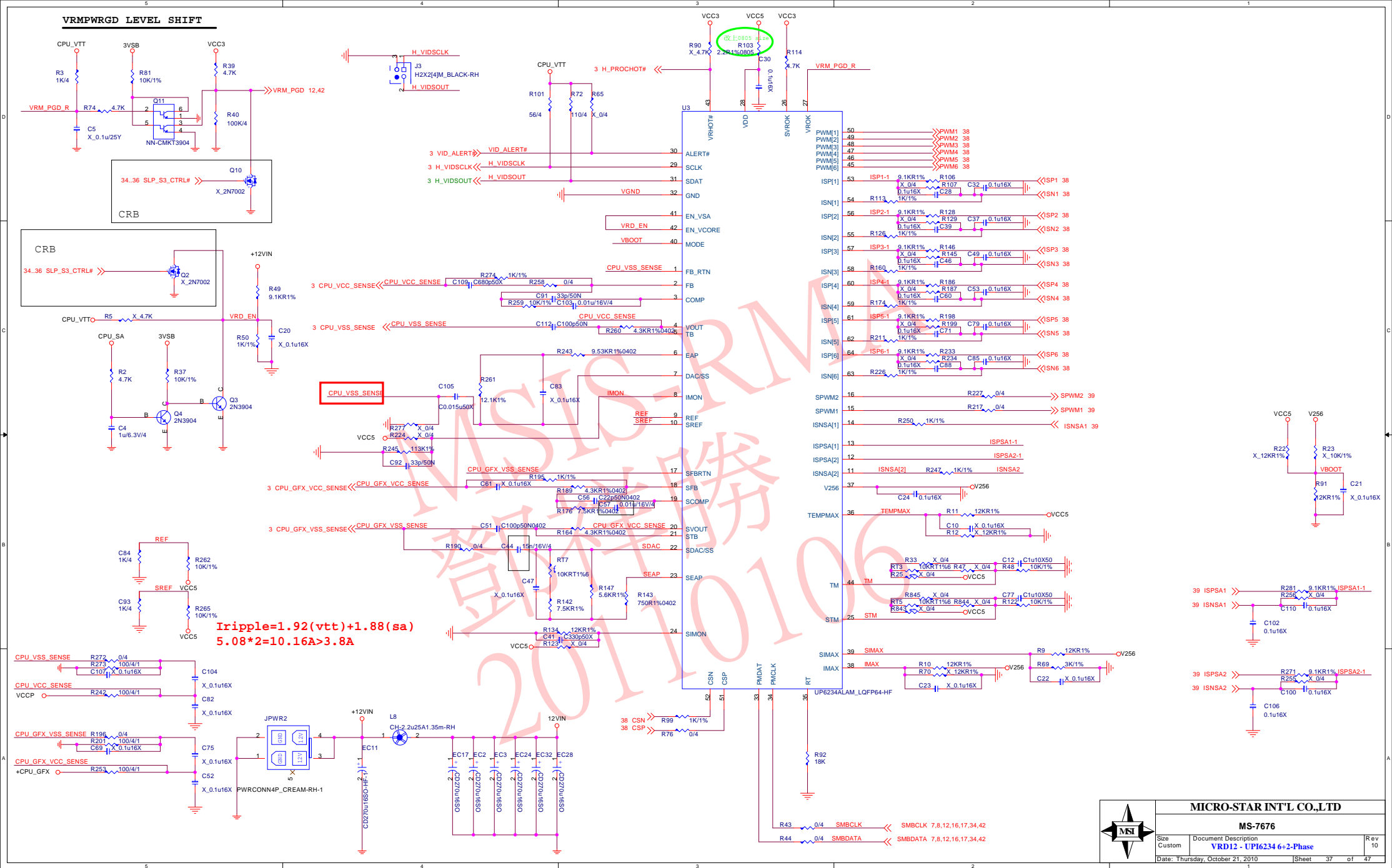
Please pull up to VCC5,
if use internal Vref.



VCCSA_VID
0 : 0.925V
1 : 0.85V



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Custom	CPU_SA - uP6113 1-Phase	10
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The diagram illustrates the PWRCONN24P_BLACK-RH-2 power connector. It features a 24-pin connector with the following connections:

- Pin 1:** 3.3V to VCC3
- Pin 2:** -12V to -12V
- Pin 3:** GND to GND
- Pin 4:** P_ON to VCC5
- Pin 5:** GND to GND
- Pin 6:** -5V to -5V
- Pin 7:** GND to GND
- Pin 8:** -5V to -5V
- Pin 9:** 5V to 5VSB
- Pin 10:** 5V to +12V
- Pin 11:** 5V to +12V
- Pin 12:** GND to GND

Additional components and connections include:

- Resistors:** R455 (10K/1%), R409 (4.7K)
- Capacitors:** C326, C316, C312, C285, C302, C257, C248
- Power Lines:** VCC3, -12V, GND, P_ON, -5V, 5V, 5VSB, +12V, VCC5
- Signal Lines:** ATX_5VSB, PSON#, ATX_PWR_OK, ATX_5VSB

POWER ON BUTTON

The diagram shows a circuit for a power-on button. A 5VSB0 pin is connected to a 1K resistor, which is then connected to a PSIN# R pin. Another 5VSB0 pin is connected to a 1K resistor, which is then connected to a PSIN# R pin. A third 5VSB0 pin is connected to a 1K resistor, which is then connected to a PSIN# R pin. The circuit is labeled 'POWER ON BUTTON'.

[illegible]

FV1

1 V1

2 V2

3 V3

4 V4

5 V5

6 V6

7 V7

PWRCONN7P BLUE

[illegible]

DPS Turbo Button

18 TURBO_MODE< 2

5

L1

L2

TURBO1

1

3

4

6

L2

TURBO_LED

+

3VSB

R314 X_1KR1%0402

R334 X_300R

6VSB

TURBO MODE#

18,41 ALL_LED_OFF# >> ALL_LED_OFF#

POWER_LED

TURBO_LED

Q29

D2

S2

G2

D1

G1

10k

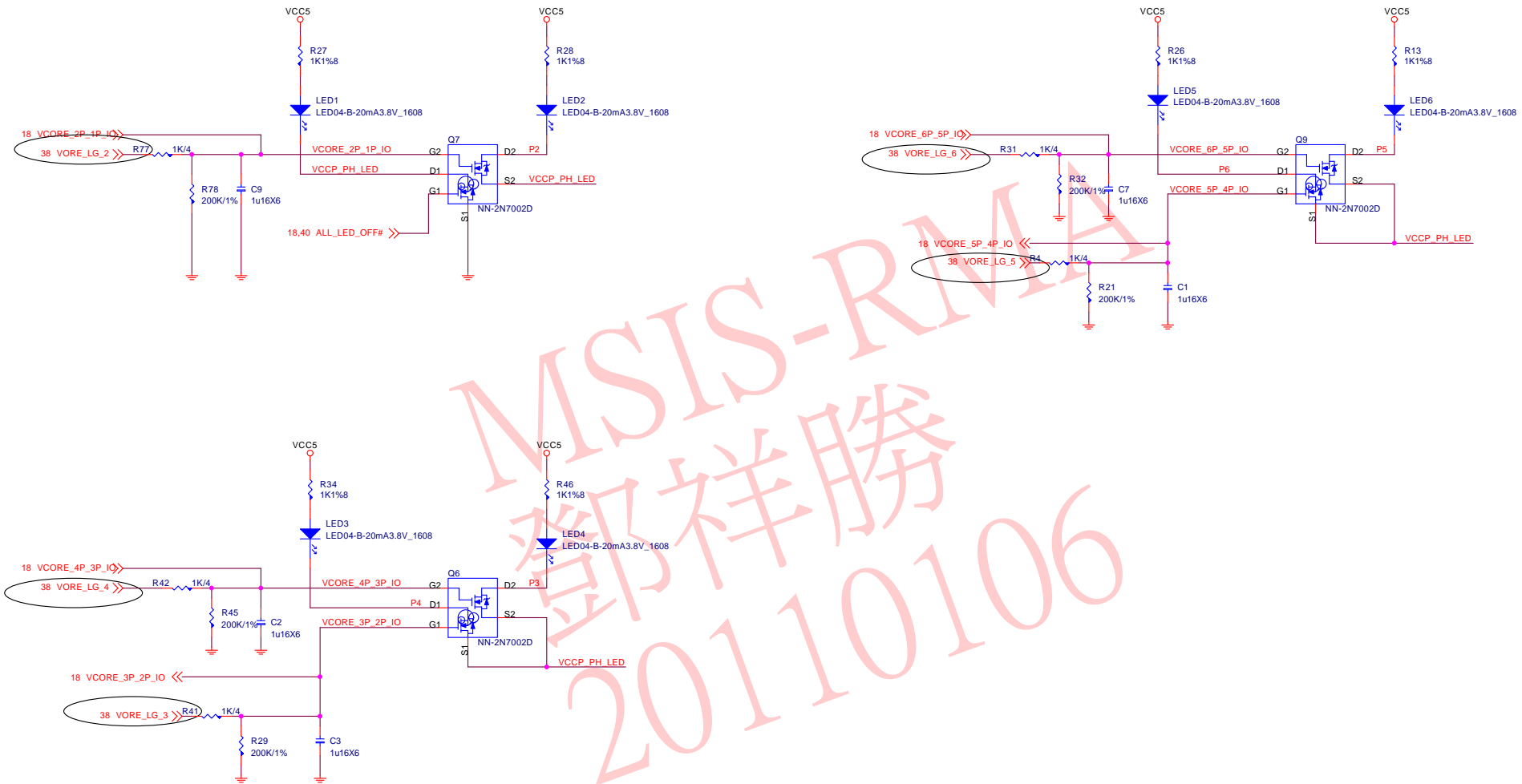
10k

NN-2N7002D



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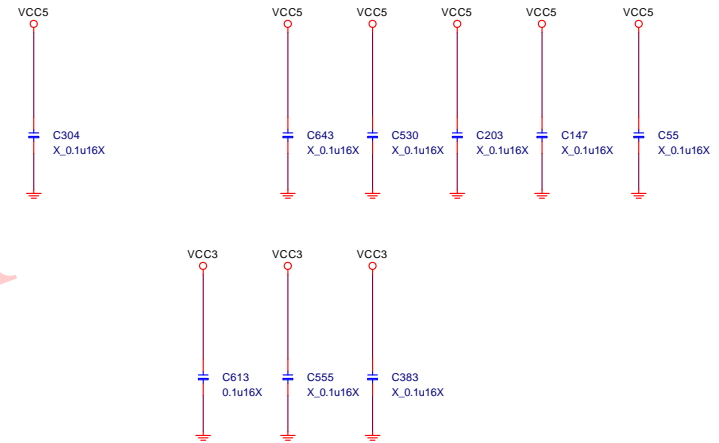
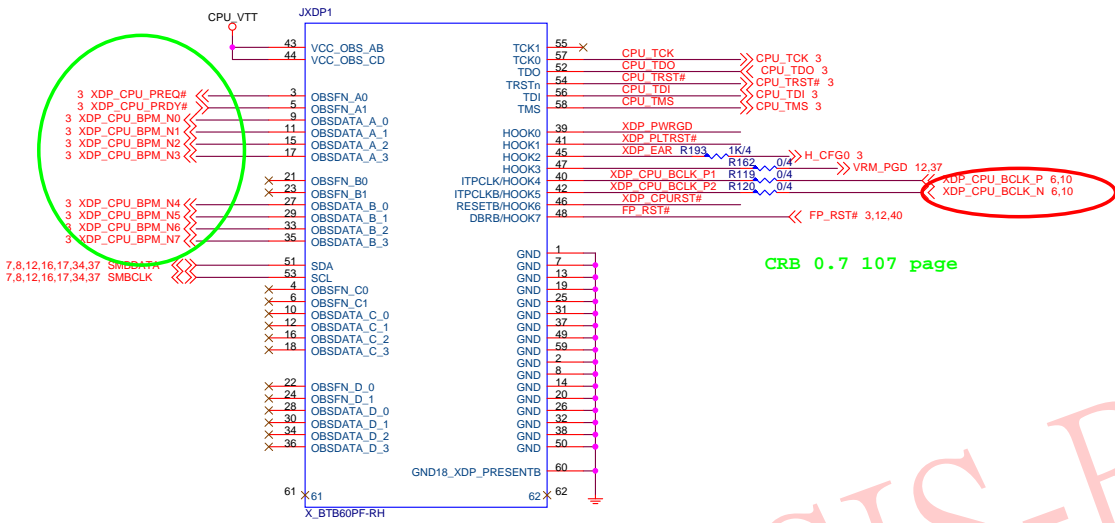
all on board LED switch



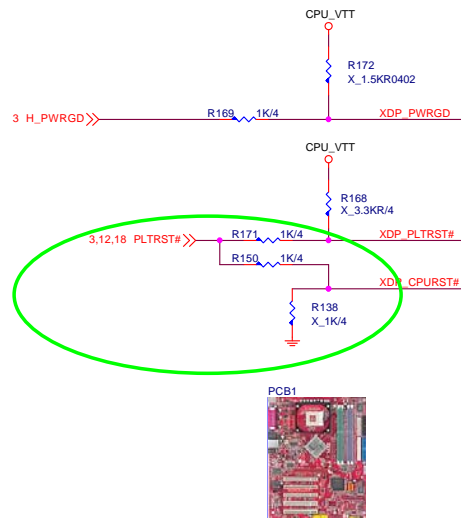
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MS-7676		
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Reserve debug port 5020

PCH XDP

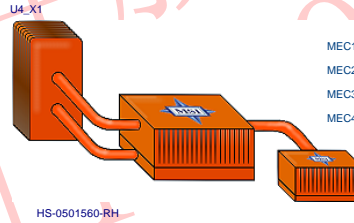


PCH XDP PWRGD/RESET



CPU_VTT
R172
X_1.5KR0402
CPU_VTT
R168
X_3.3KR/4
R171
X_1K/4
R150
X_1K/4
R138
X_1K/4

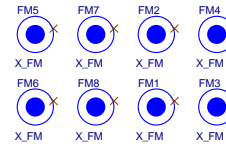
CPU Heat-pipe



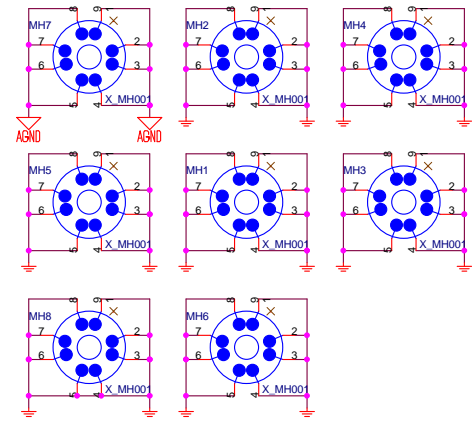
Simulation



Optical Fiducial Marks-120

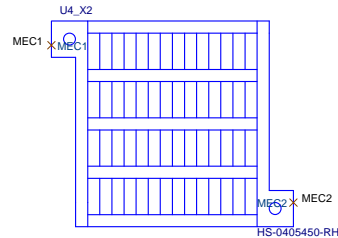


Mounting Holes



PK0-0767611-E48 競華, 27, 寶安恩斯邁廠 (MSIS)
PK0-0767611-G37, 精成, 27, 寶安恩斯邁廠 (MSIS)

Heat-Sink PCH



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